SDRAM Memory Controller

- Static RAM Technology
- 6T Memory Cell
- Memory Access Timing
- Dynamic RAM Technology
- 1T Memory Cell
- Memory Access Timing

Basic Memory Subsystem Block Diagram

- Address Decoder
- Word Line
- Memory cell
- 2^n word lines

What happens if n and/or m is very large?

Static RAM Cell

- 6-Transistor SRAM Cell
- Write:
  1. Drive bit lines (bit=1, bit=0)
  2. Select row
- Read:
  1. Precharge bit and bit to Vdd or Vdd/2 => make sure equal!
  2. Select row
  3. Cell pulls one line low
  4. Sense amp on column detects difference between bit and bit

Logic Diagram of a Typical SRAM

- Write Enable is usually active low (WE_L)
- Din and Dout are combined to save pins:
  1. A new control signal, output enable (OE_L) is needed
  2. WE_L is asserted (Low), OE_L is disasserted (High)
  3. WE_L is asserted (High), OE_L is disasserted (Low)
  4. WE_L and OE_L are disasserted.
  5. Results is unknown, don't do that!!

Typical SRAM Organization: 16-word x 4-bit

- Word 0
- Word 1
- ... Word 15
- Dout 0
- Dout 1
- Dout 2
- Dout 3
- Address Decoder
- OE determines direction
- OE Hi, Write, Low, Read
- WE_L = Write, OE_L = Read
- Double signaling: OE Hi, WE Lo

Typical SRAM Timing

- Write Timing:
- Read Timing:
Problems with SRAM

- Six transistors use up lots of area
- Consider a "Zero" is stored in the cell:
  - Transistor N1 will try to pull "bit" to 0
  - Transistor P2 will try to pull "bit bar" to 1
- Bit lines are already pre-charged high: Are P1 and P2 really necessary?

1-Transistor Memory Cell (DRAM)

- Write:
  1. Drive bit line
  2. Select row
- Read:
  1. Precharge bit line to Vdd/2
  2. Select row
  3. Cell and bit line share charges
  4. Sense (fancy sense amp)
  5. Write: restore the value
- Refresh
  1. Just do a dummy read to every cell

Classical DRAM Organization (Square)

- Row and Column Address together:
  - Select 1 bit at a time
- Row and Column Address share the same pins (A)
  - RAS goes low: Pins A are latched in as row address
  - CAS goes low: Pins A are latched in as column addresses
  - RAS/CAS edge-sensitive

DRAM Logical Organization (4 Mbit)

- Square root of bits per RAS/CAS
  - Row selects 1 row of 2048 bits from 2048 rows
  - Col selects 1 bit out of 2048 bits in such a row

Logic Diagram of a Typical DRAM

- Control signals (RAS_L, CAS_L, WE_L, OE_L) are all active low
- Din and Dout are combined (D):
  - WE_L is asserted (Low), OE_L is disasserted (High)
    - D serves as the data input pin
  - WE_L is disasserted (High), OE_L is asserted (Low)
    - D is the data output pin
- Row and column addresses share the same pins (A)
  - RAS_L-good bit: First A are matched in at row address
  - CAS_L-good bit: First A are matched in at column addresses
  - RAS/CAS edge-sensitive

DRAM READ Timing

- Every DRAM access begins at:
  1. Assertion of the RAS_L
  2. Two ways to read: early or late vs. CAS_L
- Read Access Time:
  - Early: CAS_L goes High at same time or before RAS_L
  - Late: CAS_L goes High after RAS_L
- Output Enable Time:
  - Early: OE_L goes Low at same time or before RAS_L
  - Late: OE_L goes Low after RAS_L
- Early Read Cycle Time:
  - Early Read Cycle Time = Read Access Time + Output Enable Time

Early Read Sequencing

- Assert Row Address
- Assert RAS_L
  - Commence read cycle
  - Meet Row Addr setup time before RAS/hold time after RAS
- Assert OE_L
- Assert Col Address
- Assert CAS_L
  - Meet Col Addr setup time before CAS/hold time after CAS
- Valid Data Out after access time
- Disassert OE_L, CAS_L, RAS_L to end cycle

Late Read Sequencing

- Assert Row Address
- Assert RAS_L
  - Commence read cycle
  - Meet Row Addr setup time before RAS/hold time after RAS
- Assert OE_L
- Assert Col Address
- Assert CAS_L
  - Meet Col Addr setup time before CAS/hold time after CAS
- Valid Data Out after access time
- Disassert OE_L, CAS_L, RAS_L to end cycle

Key DRAM Timing Parameters

- \( t_{RAC} \): minimum time from RAS line falling to the valid data output.
  - Quoted as the speed of a DRAM
  - A fast 4Mb DRAM \( t_{RAC} = 60 \text{ ns} \)
- \( t_{RC} \): minimum time from the start of one row access to the start of the next.
  - \( t_{RC} = 130 \text{ ns} \) for a 4Mb DRAM with a \( t_{RAC} \) of 60 ns
- \( t_{CAC} \): minimum time from CAS line falling to valid data output.
  - 15 ns for a 4Mb DRAM with a \( t_{CAC} \) of 60 ns

Early WR Cycle:
- WE_L asserted before CAS_L
- 5 ns for a 4Mb DRAM with a \( t_{RAC} \) of 60 ns
- 35 ns for a 4Mb DRAM with a \( t_{CACC} \) of 60 ns
SDRAM Memory Controller

- Static RAM Technology
  - 6T Memory Cell
  - Memory Access Timing
- Dynamic RAM Technology
  - 1T Memory Cell
  - Memory Access Timing