

**UC Berkeley  
College of Engineering  
EECS Department**

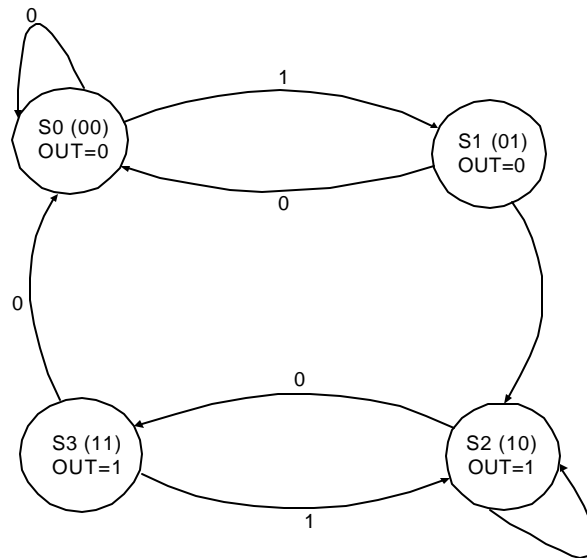
EECS150  
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Quiz #4

The last page of this quiz has the Verilog specification for a finite state machine. You may that page off, if you would like. 1) In the space below neatly draw the state transition diagram for the FSM. 2) Derive and write the logic equations for the next state and output circuitry. You do not need to minimize the logic equations.

Answer for 1)



Answer for 2)

PS <sub>1</sub>	PS <sub>0</sub>	IN	NS <sub>1</sub>	NS <sub>0</sub>	OUT
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	1	0	0
1	0	0	1	1	1
1	0	1	1	0	1
1	1	0	0	0	1
1	1	1	1	0	1

$$OUT = PS_1$$

$$NS_1 = PS_1'PS_0IN + PS_1PS_0'IN' + PS_1PS_0'IN + PS_1PS_0IN$$

$$NS_0 = PS_1'PS_0'IN + PS_1PS_0'IN'$$