

University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Sciences

EECS150
Spring 2002

J. Wawrzynek

Homework #7

This homework is due on **Friday March 15th by 1pm**. Homework will be accepted in the EECS150 box on the door to room 218 Cory Hall. Late homework will be penalized by 50%. No late homework will be accepted after the solution is posted.

1. Suppose you asked to sum the following list of 4-bit unsigned numbers (1,5,3,2,3,1), as quickly as possible using a set of carry-save adders (CSAs) and a single carry-propagate adder (CPA). You may use as many CSAs as you would like. Draw a diagram depicting the circuit you would construct. Draw each CSA and CPA as a block. Label each set of wires in-to and out-of blocks with the base 10 value of the number on that set of wires.
2. In class we discussed two different major classes of multiplier circuits, the *shift-and-add* multiplier, that multiplies n pairs of bits at a time, and the *array* multiplier, that multiplies n^2 pairs of bits at a time. These two represent different tradeoffs between cost and delay. A third class of multiplier, *bit-serial*, represents yet another tradeoff between cost and delay; it forms the product by multiplying only one pair of bits at a time. Devise and draw a circuit for a bit-serial multiplier. You may assume the presence of an external controller circuit, but need to write out the control algorithm (similar to what we did in class for the bit-serial adder). Make sure to include all necessary shift-registers in your circuit.
3. Make a table comparing *array*, *shift-and-add*, and *bit-serial* multipliers with respect cost in terms of FA cells, cost in terms of FFs, and delay, all as a function of n , the number of bits in the inputs. Use “big O” notation.
4. From Mano, exercises 4-23, 4-26, 4-27, 4-29, 4-31, 4-34, 4-38, 4-39, 4-43 & 4-44.

