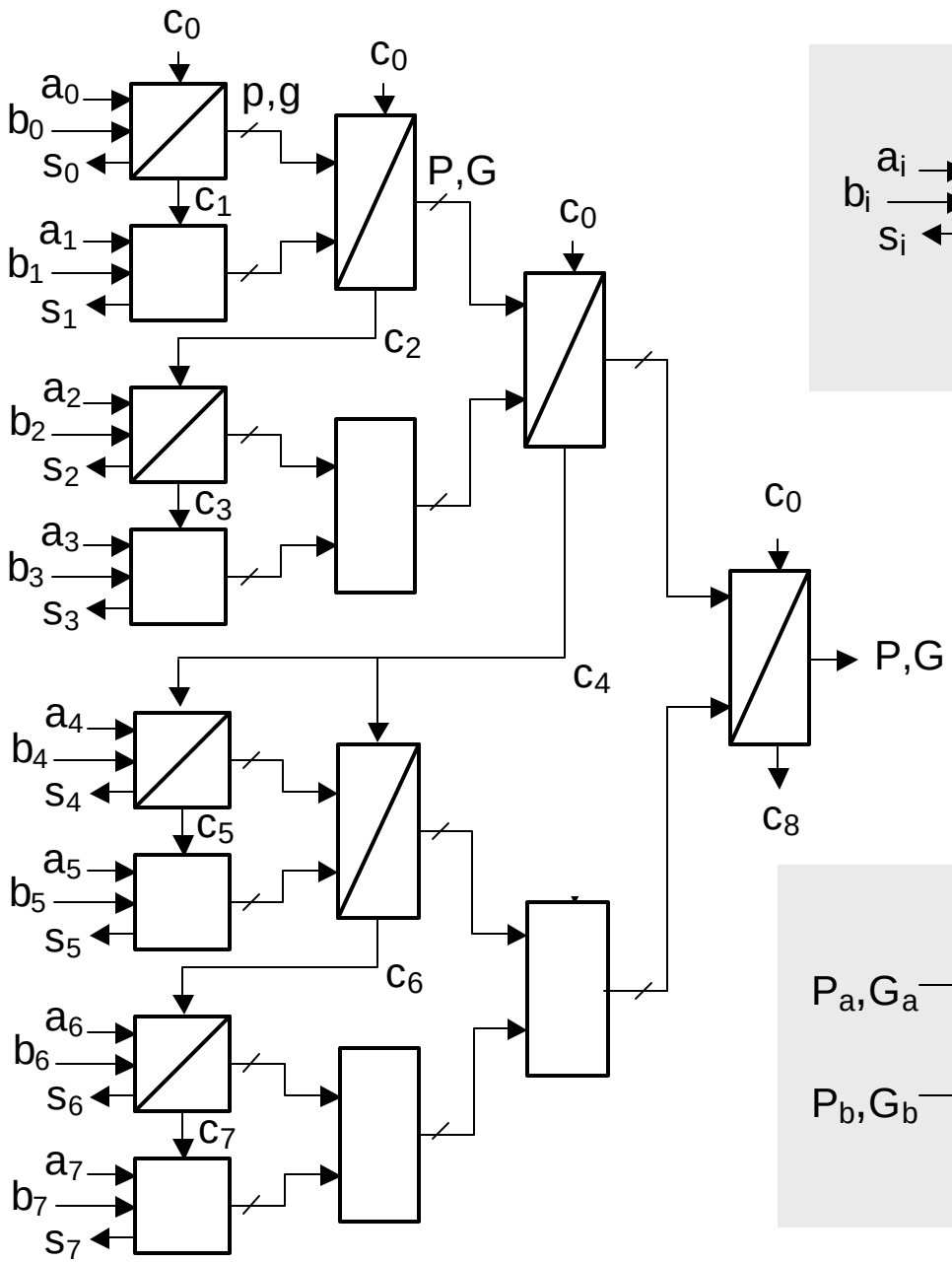
University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Sciences

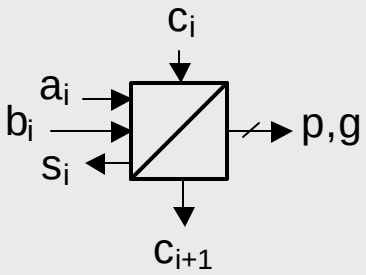
EECS150 J. Wawrzynek
Spring 2002

Homework #5

This homework is due on **Friday March 8th by 1pm**. Homework will be accepted in the EECS150 box on the door to room 218 Cory Hall. Late homework will be penalized by 50%. No late homework will be accepted after the solution is posted.

1. Below is the illustration of the 8-bit carry look-ahead adder presented in class. Draw a line on the circuit representing the critical path (signal path with worst-case delay). Using "big O" notation, how does the delay and cost scale with n for this type of adder?

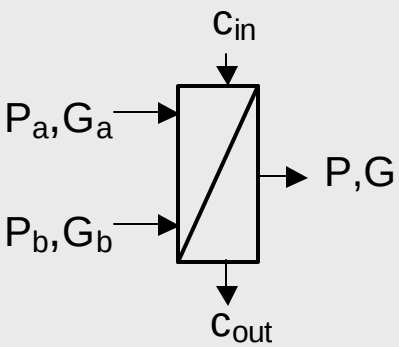




$p = a \oplus b$
$g = ab$

$s = p \oplus c_i$

$c_{i+1} = g + c_i p$



$P = P_a P_b$
$G = G_b + G_a P_b$

$C_{out} = G + c_{in} P$

2. Carry select adders.

   a) In class we discussed the carry-select adders. Assuming that the select groups are all of the same number of bits, what is the optimal size select group for a 32-bit adder?

   b) In class we also discussed the possibility of applying the carry-select idea hierarchically. The idea is that a ripple adder of n-bits can be split and implemented as a carry-select adder with group size n/2 (implemented as three ripple adders of size n/2 along with muxes). Then each of the three adders of size n/2 could be split and implemented as a carry-select adder with group size n/4, etc. By continuing the process eventually the adder size would be 1-bit and the process ends.

      Discuss the worst case delay through this adder. Again using "big O" notation, how does the delay scale with n? How does the cost (amount of hardware - number of gates or transistors) scale with n?

3. For this problem assume that your complete library of logic components comprises 2-input AND, OR, and XOR gates and inverters. Assume that inverters have cost of one unit and delay of one unit, and all other logic gates have cost of 2 units and delay of 2 units (ignore fanout and wire delay). With these assumptions, a 2-input mux would be implemented with two AND gates, one OR gate, and one inverter, and would cost 7 and have delay 5. Generate a table comparing four different adder architectures for delay and cost. The adder architectures are i) 32-bit ripple adder, ii) 32-bit carry-select adder from problem 2.a) above, iii) 32-bit hierarchical carry-select adder from problem 2.b) above, and iv) a 32-bit carry look-ahead adder based on the 8-bit carry look-ahead adder presented in class. Can you draw any conclusions from the results presented in the table?

4. From Mano, exercises 4-9, 4-10, 4-11, 4-13, 4-14, 4-15 & 4-21.