

University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Sciences

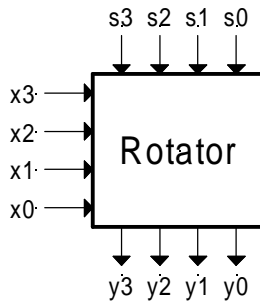
EECS150
 Spring 2000

J. Wawrzynek

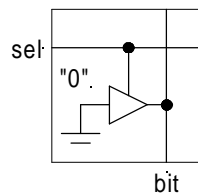
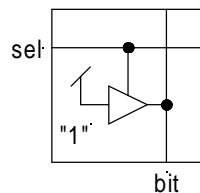
Homework #4

This homework is due on **Friday February 18th by 11am**. Homework will be accepted in the EECS150 box on the door to room 218 Cory Hall. Late homework will be penalized by 50%. No late homework will be accepted after the solution is handed out.

- Using only tri-state buffers and wires, draw the schematic diagram for a circuit that implements a *bit rotator*. The inputs and outputs are shown below. The circuit has four data inputs [x3 x2 x1 x0], four control inputs [s3 s2 s1 s0], and four outputs [y3 y2 y1 y0]. It functions as follows: The control inputs use a one-hot encoding to specify a rotate amount. For example, if [s3 s2 s1 s0] = 0001 then the output gets [x3 x2 x1 x0], if [s3 s2 s1 s0]=0010 then the output gets [x0 x3 x2 x1], etc.



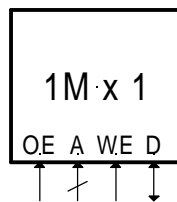
- Your task in this problem is to design the circuitry for a dual-ported 4-bit wide 4-word deep ROM. The ROM has two independent ports; each port comprises a 2-bit address bus and a 4-bit data bus. The two ports provide simultaneous access to any of the four stored data words. Begin your design process by modifying the simple single ported ROM cells shown below:



Then draw a circuit schematic for the complete dual-ported ROM including all necessary circuits. The ROM contents are shown below:

address	Value
00	0101
01	1010
10	0101
11	1010

3. Using the 1Mbit by 1 memory module shown below as a building block, draw a circuit diagram for a 4Mbit by 4 memory system. Show all necessary components.



4. In our lecture on interconnections we learned that signals traveling on wires on circuit boards and integrated circuits have a delay proportional to the square of the wire length. A common technique to shorten this delay is to *rebuffer* the signal by adding a signal buffer (usually just a pair of inverters connected in series) somewhere along the wire. Show that if we add the buffer halfway along the wire length the delay is reduced by approximately a factor of two. Ignore any delay through the buffer itself.