EECS 150 - Components and Design Techniques for Digital Systems

Lec 14 – Storage: DRAM, SDRAM

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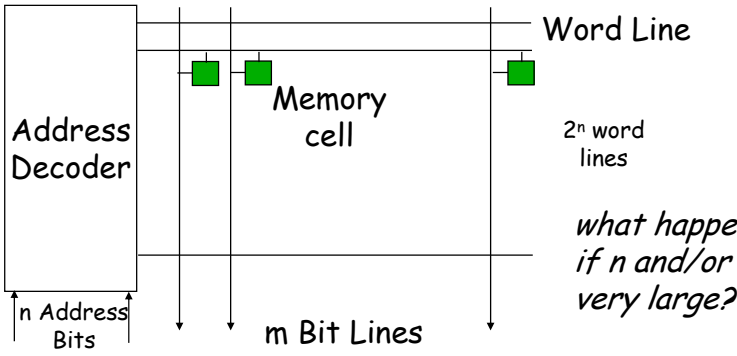
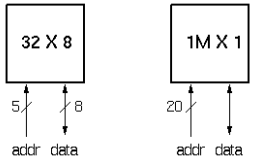
Recall: Basic Memory Subsystem Block Diagram



RAM/ROM naming convention:

32 X 8, "32 by 8" => 32 8-bit words

1M X 1, "1 meg by 1" => 1M 1-bit words

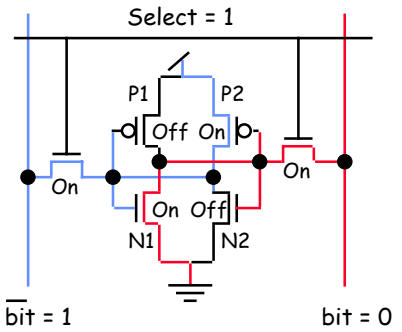


Question

- **What is the difference between a *clock signal* and a *strobe*?**

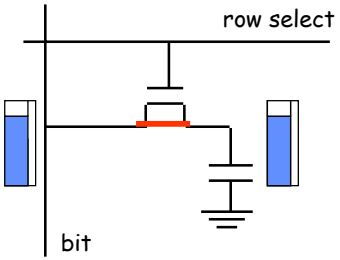
Problems with SRAM

- **Six transistors use up lots of area**
- **Consider a "Zero" is stored in the cell:**
  - **Transistor N1 will try to pull "bit" to 0**
  - **Transistor P2 will try to pull "bit bar" to 1**
- **If Bit lines are pre-charged high: are P1 and P2 really necessary?**
  - **Read starts by precharging bit and ~bit**
  - **Selected cell pulls one of them low**
  - **Sense the difference**



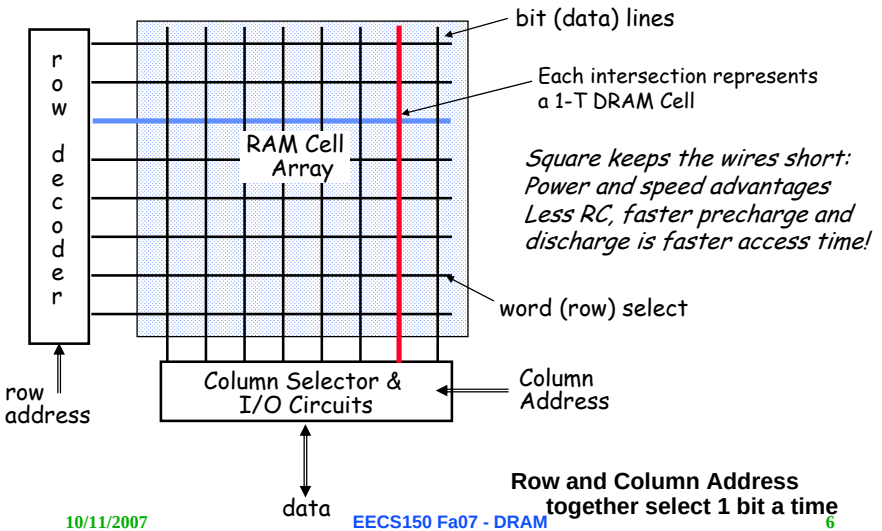
1-Transistor Memory Cell (DRAM)

- **Write:**
  - 1. Drive bit line
  - 2. Select row
- **Read:**
  - 1. Precharge bit line to Vdd/2
  - 2. Select row
  - 3. Cell and bit line share charges
    - » Minute voltage changes on the bit line
  - 4. Sense (fancy sense amp)
    - » Can detect changes of ~1 million electrons
  - 5. Write: restore the value
- **Refresh**
  - 1. Just do a dummy read to every cell. (row)



Read is really a read followed by a restoring write

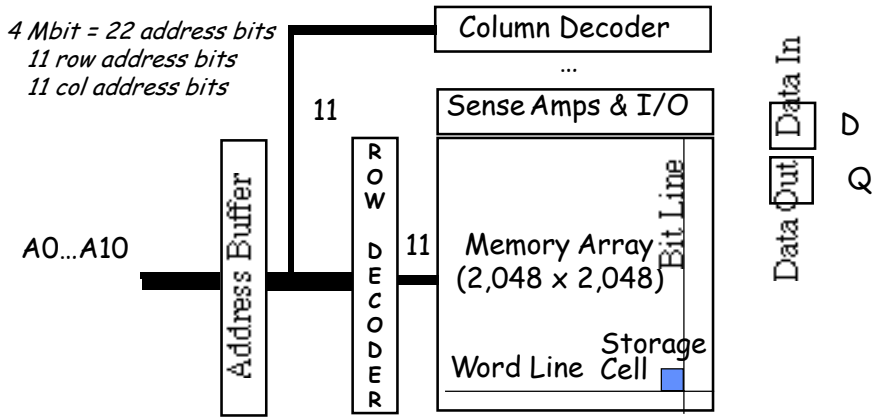
Classical DRAM Organization (Square)



Square keeps the wires short: Power and speed advantages Less RC, faster precharge and discharge is faster access time!

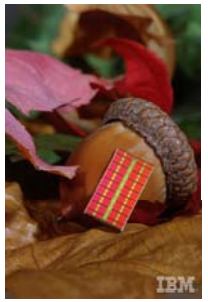
Row and Column Address together select 1 bit a time

DRAM Logical Organization (4 Mbit)



- **Square root of bits per RAS/CAS**
  - Row selects 1 row of 2048 bits from 2048 rows
  - Col selects 1 bit out of 2048 bits in such a row

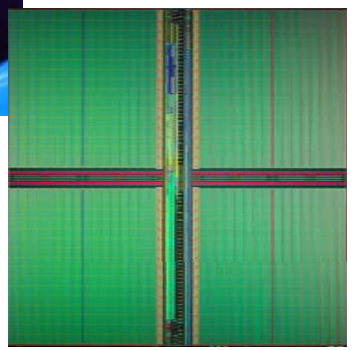
Examples



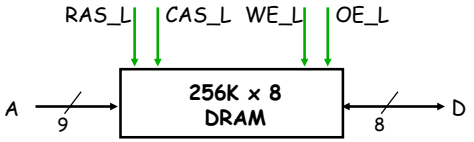
IBM 16 Mb EC/Memeory Chip

IBM 4 Mb DRAM (Dynamic Random Access Memory) chip introduced in 1989. Shown against acorn and fall foliage leaves in Burlington, Vermont where it was manufactured.

IBM 512M SDRAM Chip

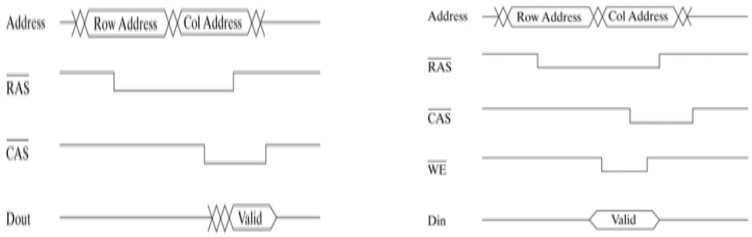


Logic Diagram of a Typical DRAM



- Control Signals (RAS_L, CAS_L, WE_L, OE_L) are all active low
- Din and Dout are combined (D):
  - WE_L is asserted (Low), OE_L is disasserted (High)
    - » D serves as the data input pin
  - WE_L is disasserted (High), OE_L is asserted (Low)
    - » D is the data output pin
- Row and column addresses share the same pins (A)
  - RAS_L goes low: Pins A are latched in as row address
  - CAS_L goes low: Pins A are latched in as column address
  - RAS/CAS edge-sensitive

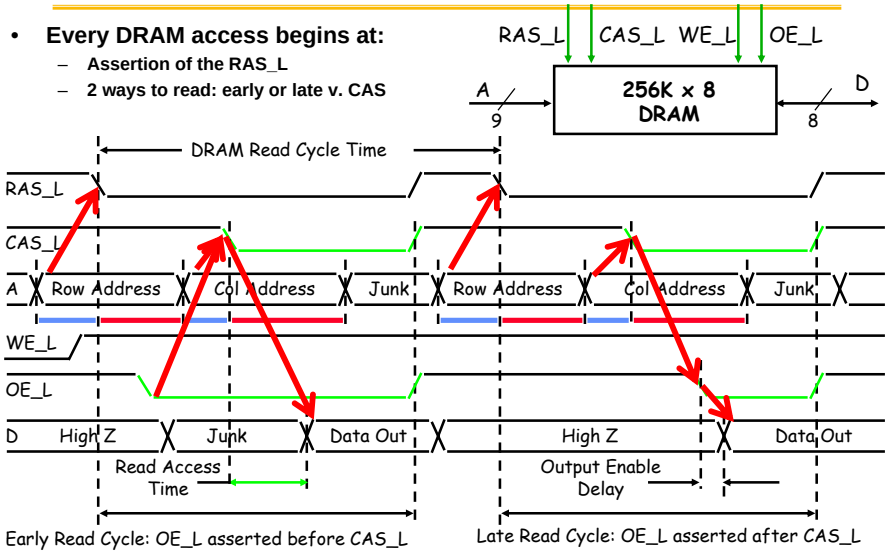
Basic DRAM read & write



- Strobe address in two steps

DRAM READ Timing

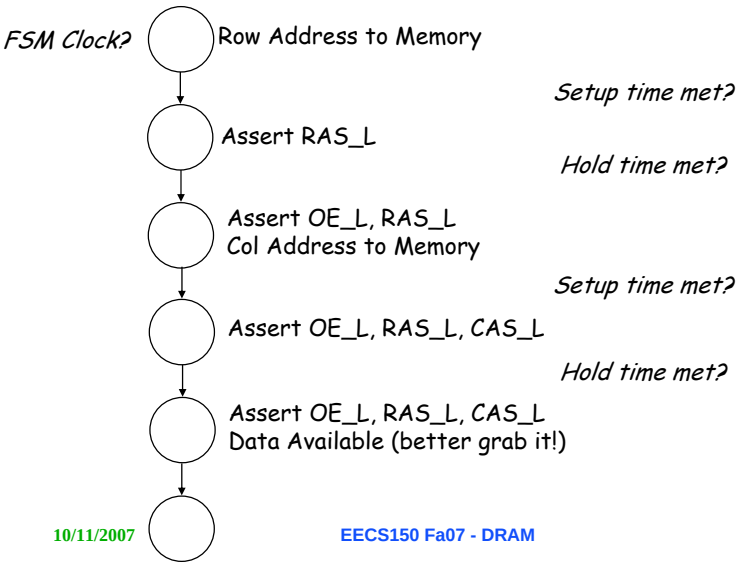
- Every DRAM access begins at:
  - Assertion of the RAS_L
  - 2 ways to read: early or late v. CAS



Early Read Sequencing

- Assert Row Address
- Assert RAS_L
  - Commence read cycle
  - Meet Row Addr setup time before RAS/hold time after RAS
- Assert OE_L
- Assert Col Address
- Assert CAS_L
  - Meet Col Addr setup time before CAS/hold time after CAS
- Valid Data Out after access time
- Disassert OE_L, CAS_L, RAS_L to end cycle

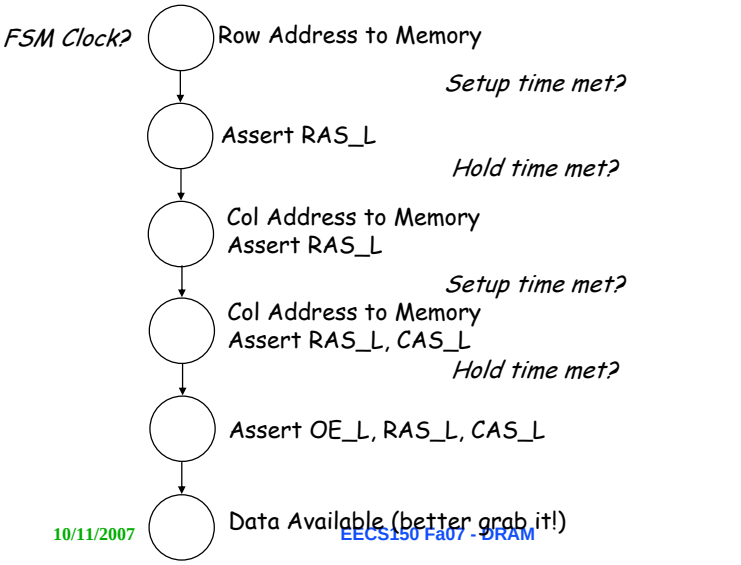
Sketch of Early Read FSM



Late Read Sequencing

- **Assert Row Address**
- **Assert RAS_L**
  - **Commence read cycle**
  - **Meet Row Addr setup time before RAS/hold time after RAS**
- ***Assert Col Address***
- ***Assert CAS_L***
  - ***Meet Col Addr setup time before CAS/hold time after CAS***
- **Assert OE_L**
- **Valid Data Out after access time**
- **Disassert OE_L, CAS_L, RAS_L to end cycle**

Sketch of Late Read FSM

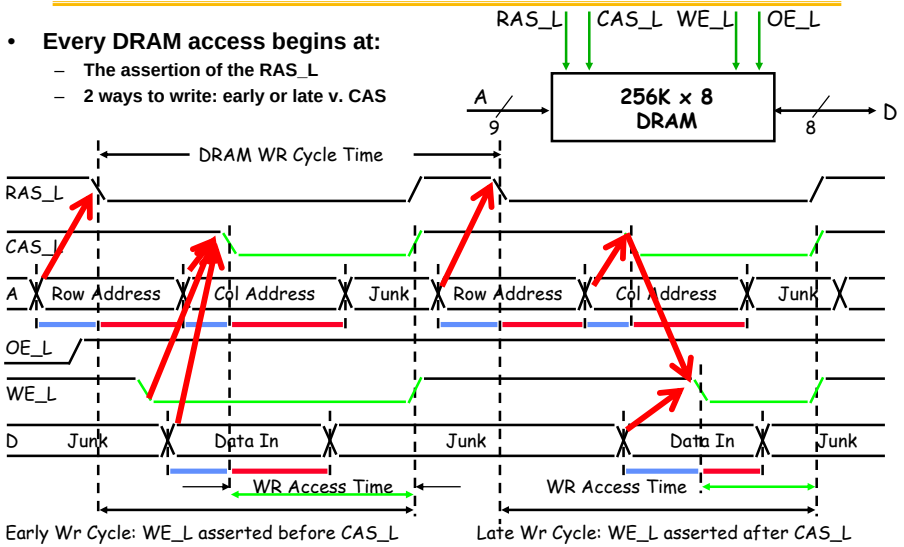


Admin / Announcements

- **Usual homework story**
- **Read: 10.4.2-3 and SDRAM data sheet**
- **We have time to understand memory protocols before using them.**
- **Proposal for a "low impact Mid III"**
  - **1 problem a day in class over 4-5 classes.**

DRAM WRITE Timing

- **Every DRAM access begins at:**
  - **The assertion of the RAS_L**
  - **2 ways to write: early or late v. CAS**

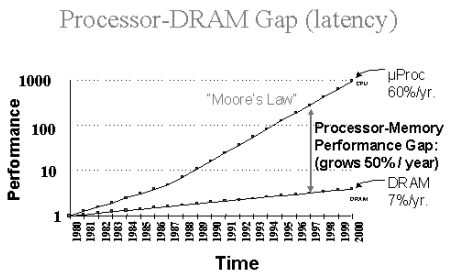


Key DRAM Timing Parameters

- t_{RAC}: **minimum time from RAS line falling to the valid data output.**
  - **Quoted as the speed of a DRAM**
  - **A fast 4Mb DRAM t_{RAC} = 60 ns**
- t_{RC}: **minimum time from the start of one row access to the start of the next.**
  - **t_{RC} = 110 ns for a 4Mbit DRAM with a t_{RAC} of 60 ns**
- t_{CAC}: **minimum time from CAS line falling to valid data output.**
  - **15 ns for a 4Mbit DRAM with a t_{RAC} of 60 ns**
- t_{PC}: **minimum time from the start of one column access to the start of the next.**
  - **35 ns for a 4Mbit DRAM with a t_{RAC} of 60 ns**

Memory in Desktop Computer Systems:

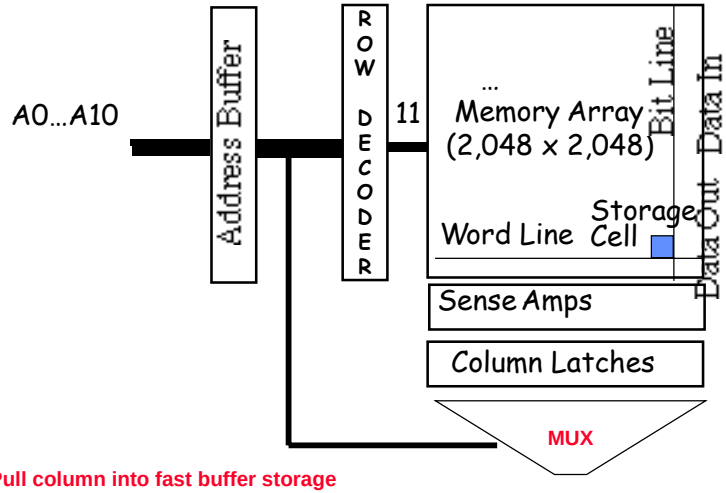
- SRAM **(lower density, higher speed) used in CPU register file, on- and off-chip caches.**
- DRAM **(higher density, lower speed) used in main memory**



Closing the GAP:

1. **Caches are growing in size.**
2. **Innovation targeted towards higher bandwidth for memory systems:**
   - **SDRAM - synchronous DRAM**
   - **RDRAM - Rambus DRAM**
   - **EDORAM - extended data out SRAM**
   - **Three-dimensional RAM**
   - **hyper-page mode DRAM video RAM**
   - **multibank DRAM**

DRAM with Column buffer



Pull column into fast buffer storage

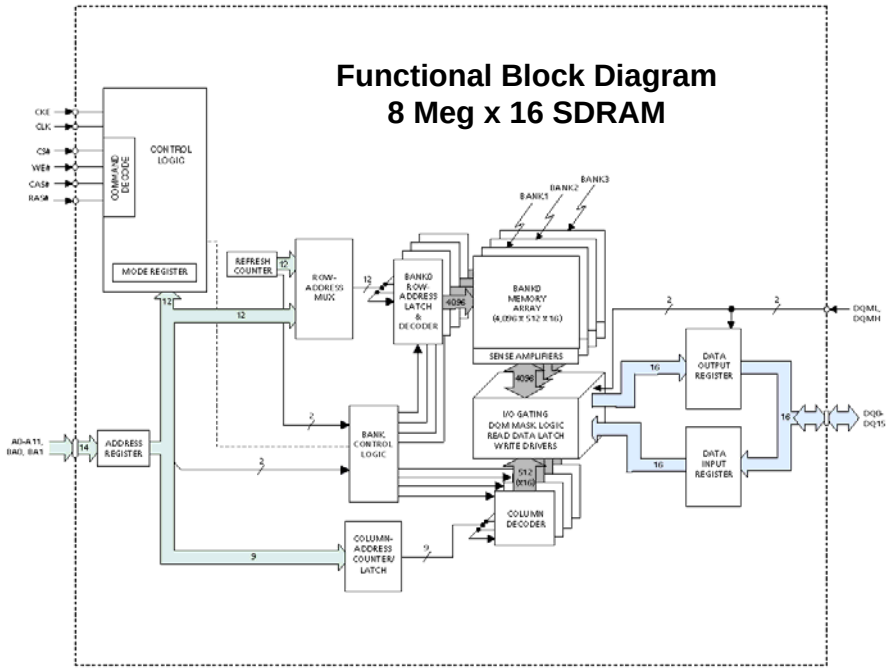
Access sequence of bits from there

Optimized Access to Cols in Row

- Often want to access a sequence of bits
- Page mode
  - After RAS / CAS, can access additional bits in the row by changing column address and strobing CAS
- Static Column mode
  - Change column address (without repeated CAS) to get different bit
- Nibble mode
  - Pulsing CAS gives next bit mod 4
- Video ram
  - Serial access

More recent DRAM enhancements

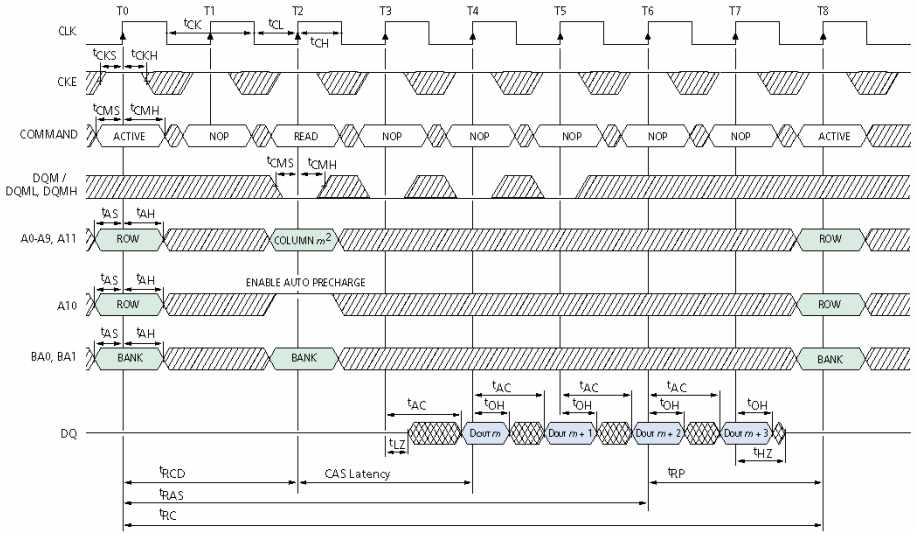
- EDO - extended data out (similar to fast-page mode)
  - RAS cycle fetched rows of data from cell array blocks (long access time, around 100ns)
  - Subsequent CAS cycles quickly access data from row buffers if within an address page (page is around 256 Bytes)
- SDRAM - synchronous DRAM
  - clocked interface
  - uses dual banks internally. Start access in one bank then next, then receive data from first then second.
- DDR - Double data rate SDRAM
  - Uses both rising (positive edge) and falling (negative) edge of clock for data transfer. (typical 100MHz clock with 200 MHz transfer).
- RDRAM - Rambus DRAM
  - Entire data blocks are access and transferred out on a high-speed bus-like interface (500 MB/s, 1.6 GB/s)
  - Tricky system level design. More expensive memory chips.



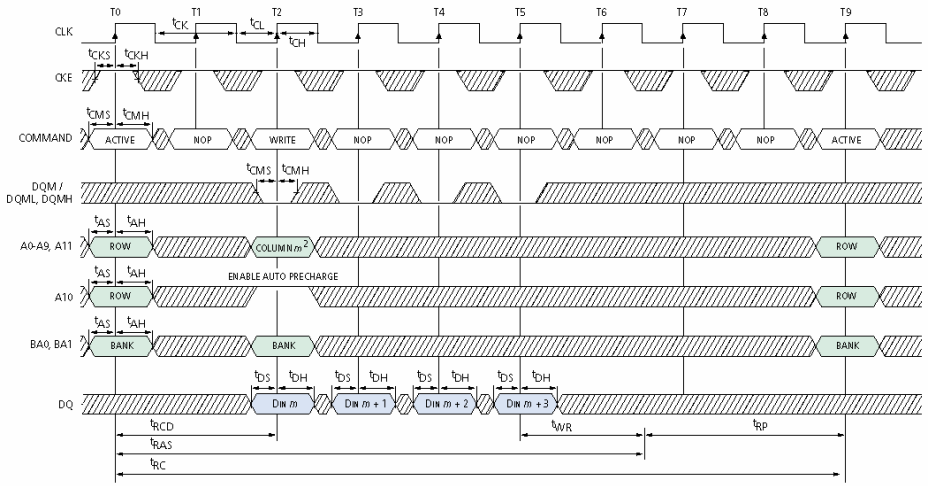
SDRAM Details

- Multiple “banks” of cell arrays are used to reduce access time:
  - Each bank is 4K rows by 512 “columns” by 16 bits (for our part)
- Read and Write operations as split into RAS (row access) followed by CAS (column access)
- These operations are controlled by sending commands
  - Commands are sent using the RAS, CAS, CS, & WE pins.
- Address pins are “time multiplexed”
  - During RAS operation, address lines select the bank and row
  - During CAS operation, address lines select the column.
- “ACTIVE” command “opens” a row for operation
  - transfers the contents of the entire to a row buffer
- Subsequent “READ” or “WRITE” commands modify the contents of the row buffer.
- For burst reads and writes during “READ” or “WRITE” the starting address of the block is supplied.
  - Burst length is programmable as 1, 2, 4, 8 or a “full page” (entire row) with a burst terminate option.
- Special commands are used for initialization (burst options etc.)
- A burst operation takes ≈ 4 + n cycles (for n words)

READ burst (with auto precharge)



WRITE burst (with auto precharge)

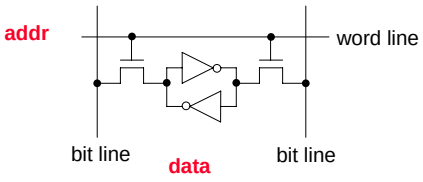


See datasheet for more details. Verilog simulation models available.

Volatile Memory Comparison

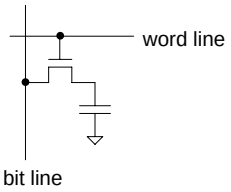
The primary difference between different memory types is the bit cell.

- **SRAM Cell**



- **Larger cell ⇒ lower density, higher cost/bit**
- **No dissipation**
- **Read non-destructive**
- **No refresh required**
- **Simple read ⇒ faster access**
- **Standard IC process ⇒ natural for integration with logic**

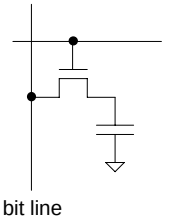
- **DRAM Cell**



- **Smaller cell ⇒ higher density, lower cost/bit**
- **Needs periodic refresh, and refresh after read**
- **Complex read ⇒ longer access time**
- **Special IC process ⇒ difficult to integrate with logic circuits**
- **Density impacts addressing**

SDRAM Recap

- **General Characteristics**
  - **Optimized for high density and therefore low cost/bit**
  - **Special fabrication process – DRAM rarely merged with logic circuits.**
  - **Needs periodic refresh (in most applications)**
  - **Relatively slow because:**
    - » **High capacity leads to large cell arrays with high word- and bit-line capacitance**
    - » **Complex read/write cycle. Read needs "precharge" and write-back**



DRAM bit cell

  - **Multiple clock cycles per read or write access**
  - **Multiple reads and writes are often grouped together to amortize overhead. Referred to as "bursting".**