UNIVERSITY OF CALIFORNIA AT BERKELEY
COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

Lab 0
Chips, Scopes, and Analyzers

ASSIGNED:	Week of 8/27
DUE:	Week of 9/2, 10 minutes after start of *your assigned* lab section.

1.0 Motivation

In this lab you will gain hands-on experience with simple combinational gates (the real version of what you met in simulation on 61C) breadboarding simple circuits and using the basic tools of hardware design – signal generators and oscilloscopes.

In future labs, you will be "wiring up" circuits by programming your FPGA. This lab will give you a little bit of experience with traditional gates and insight toward what is going on inside the FPGA. Also, in debugging hardware you will often resort of using (or building) tools that generate certain patterns and observing how your hardware behaves when presented with those patterns.

2.0 Introduction to TTL

In this lab you will use a single 74C00 quad NAND gate in a Dual Inline Package (DIP). You will gain some experience using the tools on your lab bench. First, we will use the power supply and multimeter to observe the combinational behavior of a simple chip. Using the four gates that come in a 7400 package, you'll build and verify a simple combinational circuit. Second, we will utilize the function generator and oscilloscope to observe its timing behavior. Third, we will "break the rules" for combination logic and build a simple sequential circuit – a ring oscillator – by creating a cycle of combinational logic. Finally, we'll build a sequential circuit that is useful for synchronous digital logic design – a latch.

3.0 Prelab

There is no prelab preparation for this lab. Your TA will explain the operation of the materials described below. You will consult the associated documentation as you work through the lab.

Materials

1. Breadboard
2. HP 8116A Pulse/Function Generator
3. HP 54645D Mixed Signal Oscilloscope
4. HP E3630A DC Power Supply
5. 74C00 quad NAND chip
6. Probes

4.0 Lab Procedure

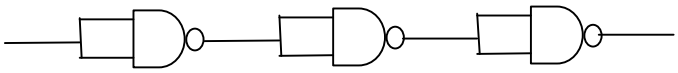
Receive you CS150 account from your lab TA. Log in and verify that your account works.

(A) Logical Behavior

1. Go on the web and find the datasheet for the chip that you are using. Identify the pins used for power and ground, as well as the inputs and outputs of the gates.
2. Configure your power supply to provide 5V DC. Use the red COM terminal for ground. Note that this connection may not be present on some power supplies in which case the ground should be connected to the corresponding negative terminal. Verify with your multimeter that you have a 5V supply to work with before you wire it to your chip. Wire these to Vdd and GND rails of your breadboard. Wire the rails to the corresponding Vdd and Gnd pins of your 74C00.
3. Pick a NAND gate in your 74C00, identify its input pins and its output. Connect GND to the inputs of the NAND gate and capture the output using the multimeter. Repeat for the other 3 combinations of high and low inputs for the NAND gate and draw the truth table. Verify that it is the NAND function. (You can also use your oscilloscope to observe the signals.)
4. Using multiple NAND gates, configure them to implement a 2-input XOR function. Draw the circuit. Draw the truth table. Wire it up and verify that it works. Have your TA initial your checkoff.

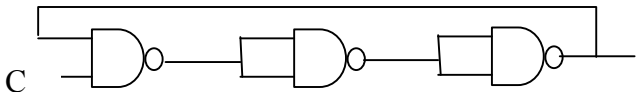
(B) Timing behavior

1. Use the pulse/function generator to create a square wave as input to the series of NAND gates. You may need to play around a little with the amplitude and offset for some of the function generators to get a proper square wave oscillating from 0V to 5V. If you are not familiar with the operation of the oscilloscope, read the summary below. Adjust the triggering and timescale so that you can see a complete cycle. Adjust the cursors so that you can read the period on the screen (press the cursors button, and then select the time/measurement cursors before using the entry knob to move them to their proper location).
2. Wire your NAND gates to form a sequence of inverters.
3. Capture the input, the output of the first gate and the output of the last gate using the oscilloscope.
4. Use the oscilloscope to measure the rise and fall times and the propagation delays in your circuit. Use the time and voltage cursors to get these measured times.
5. Find the rise and fall times and the propagation delays described in your datasheet? How do these compare to your measurements?
6. Reconfigure your circuit to have a single NAND gate driving three gates. How do the propagation times change?



(C) Simple Sequential Circuit with Feedback

1. Configure your circuit to form a ring containing three NAND gates.
2. Explain the expected behavior of this circuit.
3. Estimate the period and frequency of the output
4. Capture the waveform and compare with your estimate. Have you TA initial your checkoff.

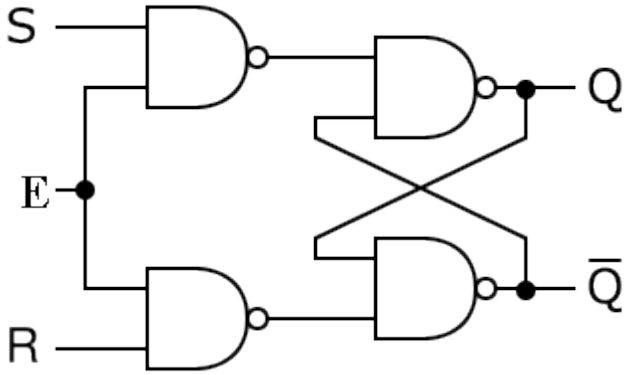


(D) Simple Latch

1. Configure your circuit to form a gated SR latch with cross-coupled NAND gates. hint: http://en.wikipedia.org/wiki/Latch_(electronic)
2. What should be the behavior when the "Clock" input is high?

3. What should be the behavior when the "Clock" input is low?

4. Capture the waveform showing that it works as a latch. (You will need to think a little bit about what you are going to provide as inputs to demonstrate it behavior to your TA.)


S
E
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5.0 HP54645D Mixed Signal Oscilloscope (Logic Analyzer)

Figure 1: HP54645D Mixed Signal Oscilloscope

Shown in Figure 1 above, is the HP54645D Mixed Signal Oscilloscope, which we will generally refer to as simply "the oscilloscope" or "the logic analyzer." It is in fact a combination of these instruments, both of which are design to graph waveforms (analog and digital respectively) over time.

Using the logic analyzer is significantly less complicated than it appears and it is an invaluable debugging tool. The logic analyzer allows us to examine signals over time at various scales, you can zoom in to see events on different clock cycles, or zoom out to see how a signal behaves over the course of seconds.

5.1 Front Panel Controls

This section will explain at least a little bit about all of the buttons and controls on the front panel of the logic analyzer.

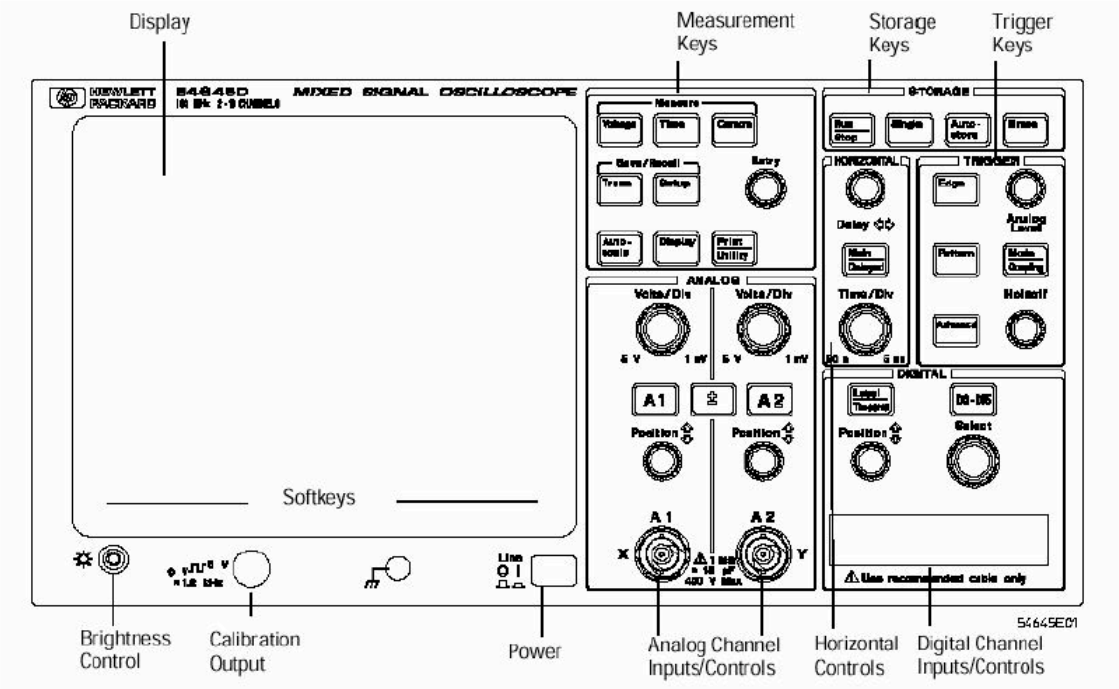

Figure 7: HP54645D Front Panel Controls

5.1.1 Display & Brightness Control

Of course this is the screen, where you will see your waveforms and other such information. At the bottom left of the screen is a brightness control. If your screen appears blank, try the brightness.

Notice the row of softkeys across the bottom of the screen.

5.1.2 Softkeys

In order to provide more advanced controls without cluttering the front panel, there are six softkeys, whose meaning changes as you navigate the controls menus or change operating modes. If we mention a button that does not appear on the front panel, check the softkeys.

5.1.3 Calibration Output

This is used to calibrate the analog oscilloscope probes. If you are in doubt as to whether the probe is behaving correctly, hook it to the calibration output and hit **Autoscale**. You should see a nice clean 0-5V square wave at ~1.2kHz.

5.1.4 Autoscale

Located in the **Measurement Keys** section of the front panel, this is one of the most used buttons. It will cause the oscilloscope/logic analyzer to automatically search for signals on its inputs. When it finds signals it will attempt to place them in the middle of the screen and set the triggering to that they are stable and ready for use.

If you lose the signal, **Autoscale** may help.

5.1.5 Measurement Controls

Consists of three buttons; **Voltage**, **Time**, and **Cursors**. **Voltage** and **Time** will display options for types of measurements (V_{avg}, V_{p-p}, Freq, etc.) on the softkeys. When selected, the measurements will be displayed at bottom of screen. The **Source** softkey can be used to select the correct analog source channel.

The **Cursors** button is used to display or clear time and voltage measurement cursors which are selected with softkeys and moved with the **Entry** knob. Note that you can have the time cursors print out the value (in Hex, Binary or Decimal) of the 16 digital channels.

5.1.6 Analog Controls

The **Volts/Div** knob can be used to change the vertical (voltage) scaling of the two analog channels. Notice that there are two knobs: the scaling for each of the two channels are separate (1 division may be 1V on A1 and 2V on A2).

The **A1** and **A2** keys will turn the respective analog channel on or off while bringing up a softkey menu allowing you to select AC or DC coupling and Noise Filtering. The ± button will allow you to see sum and difference waveforms.

5.1.7 Horizontal

The **Delay** knob will allow you to scroll the screen left or right.

Main Delayed: Horizontal mode should be set as normal with softkeys, the **Time Ref** softkey controls what reference to use when zooming in with **Time/Div** knob. **Vernier** is used to minimize time steps in **Time/Div** knob.

Time/Div changes the time per grid block. The time/div scaling is displayed at the top of the screen.

5.1.8 Digital

The **Label/Threshold** button allows you to label any of the 16 probe leads of the logic analyzer. The **threshold** menu and softkeys let you choose what type of logic you are using, MOS or TTL should work fine.

The **D0-D15** button allows you to select which logic analyzer probes will be displayed. Individual signals can be selected with **Select** knob and turned on or off with the softkeys.

The **Position** knob will let you reorder the signal on the display. Notice that this will affect the value readout produced by the time cursors (see 5.1.5 Measurement Controls).

5.1.9 Trigger

The **Edge** button will select edge triggering mode, where the scope will wait for a rising or falling edge (selectable with softkeys) on the channel you select using the softkeys.

The **Pattern** button will let you modify the pattern triggering mode pattern, where the scope will trigger on a pattern of High, Low, Rising, Falling or Don't Cares on the various inputs. Use the **Select** knob and softkeys to set the pattern.

The **Analog Level** knob will let you set the analog voltage at which to trigger (applies to the analog signals only). The **Holdoff** knob will allow you to set the amount of time before the screen is redrawn; you will want to set this to the minimum.

The **Mode/Coupling** button will bring up a softkey menu of triggering modes: **Auto Level**, **Auto** and **Normal**. While **Auto** may be useful for analog work, you will always want **Normal** for using the logic analyzer.

The **Advanced** button brings up a softkey menu of the various triggering modes.

5.1.10 Storage

The **Run/Stop** button starts and stops the refresh on the display. This is useful when you want to freeze the screen to examine it more closely.

The **Single** button can be used to set the scope to single mode, where it will trigger once, remember the data and then freeze the screen. This is perfect for capturing a one time event, like something that happens at reset.

Erase will clear the screen; measurement should be restarted with the **Run/Stop** button.

5.2 Triggering

Triggering the logic analyzer properly is key to being able to actually see the waveforms you are interested in. We recommend that you become intimately familiar with the various triggering modes, but perhaps the most useful for digital work is pattern mode. This section is a brief tutorial on how to set up and use pattern triggering mode.

1. Make sure the logic analyzer is on
2. Make sure the **channels you are interested in** are showing
    a. The **A1** and **A2** buttons can be used to enable or disable the analog channels.
    b. The **D0-D15** button and **Select** knob will let you select specific digital signals. You can then use the **softkeys** to enable or disable them.
3. Switch the logic analyzer to **Normal triggering mode**.
    a. Press **Mode/Coupling** in the **Trigger Box**
    b. Select **Normal** under **Trigger Mode** on the softkey menu
4. Switch the logic analyzer to **Pattern advanced triggering mode**.
    a. Press **Advanced** in the **Trigger Box**
    b. Select **Pattern** under **Advanced Trigger Mode** on the softkey menu
5. Set up a triggering pattern
    a. Press **Pattern** in the **Trigger Box**
    b. Use the **Select** knob to select a signal
        i. Select the value that signal should have
        ii. Note that each signal is compared against its bit in the pattern, when all 18 (16 digital, 2 analog) channels match, the scope will trigger
        iii. L: Logic Low
        iv. H: Logic High
        v. X: Don't Care (Ignore this signal for the pattern)

vi. ↑: Rising Edge
vii. ↓: Falling Edge

6. Set the **Time/Div**
   a. Play with the **Time/Div** knob until the time per division is approximately what you need.
   b. Remember a 27MHz clock cycle is 37ns from rising edge to rising edge.

7. Start the logic analyzer running
   a. To trigger once and save the waveforms press **Single**
      i. If you want to trigger again you will need to press **Single** again
   b. To trigger every time the pattern is matched press **Run/Stop**

6.0 Lab 0 Checkoff

Name: _____
Section: _____

ASSIGNED:	Week of 8/27
DUE:	Week of 9/2, 10 minutes after start of *your assigned* lab section.

I	NAND truth table/waveform	_____
II	XOR truth table/waveform	_____
III	Tr, Tf, Tp0-1, Tp1-0	_____
	_____ _____ _____ _____	
IV	Ring oscillator	_____
V	D-Latch	_____
VI	Hours Spent:	_____
VII	Total:	_____
VIII	TA:	_____

RevD – 8/28	Shah Bawany	Minor change to power supply usage description
RevC – 8/28	Culler	Additional explanation of steps.
RevB – 8/27/2007	Udam Saini	Updated to explain/modify some of the lab steps. Copied a detailed description of the Oscilloscope that was in an old lab.
RevA	Culler	Draft of basic lab