University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Science

EECS 150 D. E. Culler
Fall 2007

Homework #6:
Assigned 10/11/2007, Due 10/19/2007 at 2 PM

Problem 1: The follow memory units are specified by the number of "words" times the number of bits per word. How many address line and input/output data lines are needed in each case? How many bytes are stored in the memory units?

a. 2G x 8
b. 16M x 32
c. 256K x 64

Problem 2. You are to build a memory system out of the ST microelectronics M68AW256M SRAM chips, which have the logic diagram is shown below. It should contain 1 G word, where each word is 32 bits in length. It should be possible to read and write bytes, half-words, and words, but only on boundaries that are a multiple of the object size (ie., half-words have to be half-word aligned, words have to be word aligned). Draw the circuit diagram for the memory system using this chips and what additional gates that you require.

Figure 2. Logic Diagram

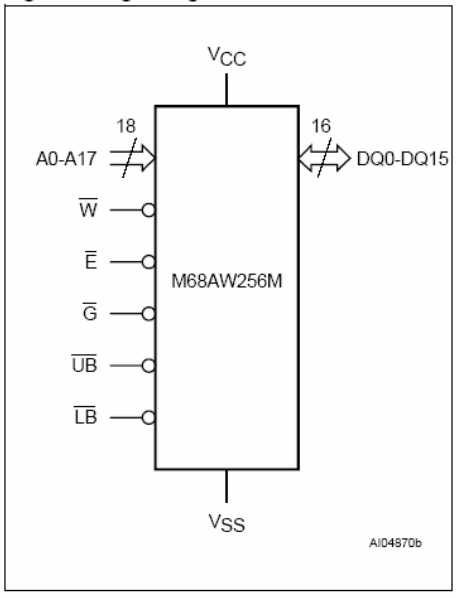


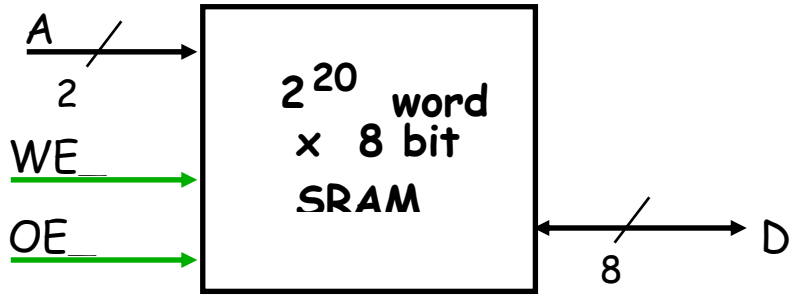
Table 1. Signal Names

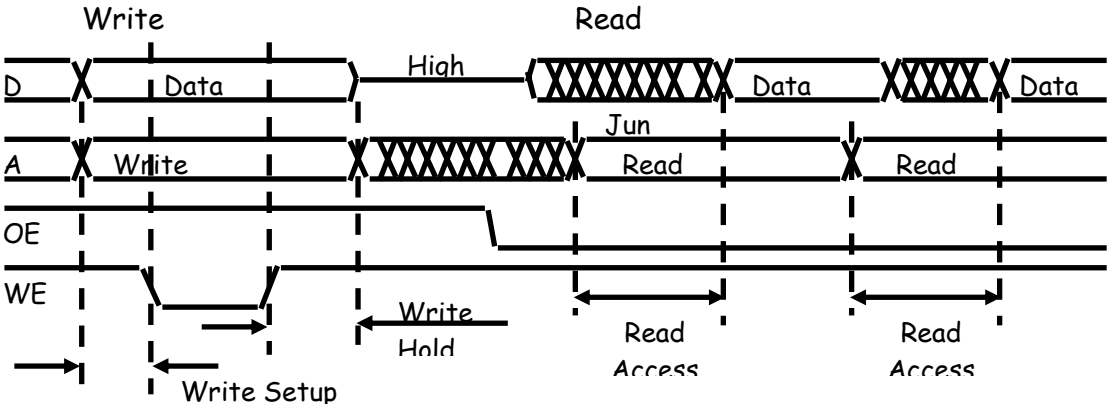
A0-A17	Address Inputs
DQ0-DQ15	Data Input/Output
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{UB}$	Upper Byte Enable Input
$\overline{LB}$	Lower Byte Enable Input
V_{CC}	Supply Voltage
V_{SS}	Ground
NC	Not Connected Internally
DU	Don't Use as Internally Connected

Problem 3: Show how to implement a 3-input, 8-output decoder by giving the truth table and logic diagram using 2-input NAND and NOR gates. (Can you do better than the obvious?)

Problem 4: Draw a block diagram for a 256 x 4 SRAM that has a square aspect ration, i.e., and equal number of rows and columns. How are the address bits used?

Problem 5: You are to implement a controller to read and write the following 1 MB SRAM memory. The Read Access time is 17 ns. The Write Setup is 7 ns. The Write Hold time is 3 ns. The clock rate of your FSM is 25 MHz. Your FSM also controls a memory address register (MAR) and a memory data register (MDR). It has a READ input, a WRITE input, and a DONE output. On a read, it should capture the address in the MDR, cause a memory read, capture the result in MDR and signal DONE. On a write it should capture the address in MAR and the data in MDR, perform the write, and signal when it is complete. Draw the memory datapath consisting of the MAR, MDR, SRAM and associated control and data lines. Diagram your controller and how it interfaces to the datapath. Show the state transition diagram for your memory controller. Write out STD in verilog. (Hint, how many cycles do you need to wait at each step?)





Problem 6: You are to build a 256k x 32 memory system out of the DRAM chips that are illustrated in Lecture 14, Slide 11. However, you are going to borrow and idea from RAMBus and use a fast narrow data link. Even though the memory system is 32-bit wide, each time we read a word we will receive it a byte at a time, four bytes on consecutive cycles. Assume the read access time is 60 ns, the read cycle time is 110 ns, and the Output Enable Delay is 10 ns. Further assume that your controller logic is running on a 10 ns clock. How many cycles does it take to complete a word read? How many cycles before the next one can start. Diagram the memory system organization with only an 8-bit link between the memory chips and the MDR.