1. **Address** | **Label** | **Instruction** | **Operands** | **Comments**
--- | --- | --- | --- | ---
3 | RDI0 | DO | SELPC, Sel2 = Bus1, Load_ADCt | ADDR < PC, NPE < R0, Pk+1 → PC (controller uses Do for Write) |
4 | RDI1 | DO | Load_ADDRED, Inc_PC | SELz = Hw, Load_d0t, Instruction Fetch < dispatch > |
5 | RDI2 | JMP | | |

2. **Address** | **Label** | **Instruction** | **Operands** | **Comments**
--- | --- | --- | --- | ---
6 | DJNZ0 | DO | SELPC, Sel2 = Bus1, Load_ADCt | ADDR < PC, R0 < PC, Pk < Pk+1 |
7 | DJNZ1 | DO | Load_ADDRED, Inc_PC | SELd0t, ALUout = IN - 1, RegZ & alu zero flag, Load_d1t, Sel2 = ALU, Load_d0t |
8 | DJNZ2 | JMP | If 'Z' flag, Then Instruction Fetch, Then < dispatch > |
9 | DJNZ3 | | If 'Z' flag, Then Instruction Fetch, Then < dispatch > |
10 | DJNZ4 | DO | Sel2 = Hw, Load_PC | PC < RAM [ADD_R] |
11 | DJNZ5 | JMP | Instruction Fetch, < dispatch > |

*Changes to MCU: (0) SELsrc with SELd0t for MVP1
(1) add Load_d2t to ALUout = IN - 1

3. **Diagram**

CLK

μPC

μPC LD

OUT

OUT CE
4. \[ SAE_{u+1} = SAE_u + (I_1 - I_2) + (I_3 - I_4) \]

\[ \text{throughput} = \frac{1}{T} = \frac{1}{(t_{\text{add}} + t_{\text{amp}})} = \frac{1}{(10us + 5us)} = \frac{1}{15us} = 66.7 \text{ MHz} \]

\{atency\} \text{ makes 4 clock cycles}