CS152 Section 3

Q1. Precise Exceptions

- Describe how program execution time may be affected by adding support for precise exceptions.
    - Remember, execution time = instructions/program * cycles/instruction * time/cycle
- Compare and contrast precise exception handling with branch misprediction

Q2. Cache Organization

Consider a 1 KiB 4-way set-associative cache with 32-byte cache lines. The address is 12 bits wide. How are the address bits partitioned?

- Tag:

- Index:

- Offset

Q3. Replacement Policies

Suppose we see the following stream of accesses where A, B, C, D, and E represent unique addresses from different lines that all map to the same set:

A, B, C, D, B, A, E

Assume the cache has four ways and all lines in the set are initially invalid. When address E is accessed, one of the cache lines must be evicted. For each replacement policy, which line gets evicted?

- FIFO

Way0	Way1	Way2	Way3	Policy State after request

- NMRU

Way0	Way1	Way2	Way3	Policy State after request

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Q4. Cache Optimizations

For each technique, indicate whether implementing it will **increase**, **decrease**, or have **no change** on each aspect.

Technique	Hit Time	Miss Penalty	Miss Rate	Hardware Complexity
Smaller, simpler caches				
Multi-level caches				
Smart replacement policy				
Pipelined writes				
Write buffer				
Sub-blocks (sector cache)				
Code optimization				
Compiler prefetching				
Hardware prefetching (stream buffer)				
Victim cache				