CS152 Section 9

Q1: Vector Programming Lane Tradeoff

Suppose we want to add two vector registers (add v1, v2, v3), followed by another addition to different registers (add v4, v5, v6). The next instruction after that uses a different functional unit. VLR=MAXVL=32. What would you choose between an ALU with 8 lanes and 2 cycles dead time, and an ALU with 16 lanes and 8 cycles dead time? *To reduce the complexity of control logic, some vector machines require some recovery time or dead time in between two vector instructions dispatched to the same vector unit.*

Q2: Vector v.s. Packed-SIMD

What are the distinguishing features between a vector architecture and a packed-SIMD architecture? List the advantages of each.

Distinguishing feature:

Vector architecture:

Packed-SIMD: