Fall 2005			EE 40 Lecture Plan Version 11/14/05		Prof. Neureuther
Wk	**#**	**Date**	**Lab**	**Topic**	**Reading**
1	1	29-Aug	Orientation	Energy and Information, Basic Boolean	1.1, 7.1-7.3 to pp 340
	2	31-Aug		Charge, Current, Voltage, Power	1.2-1.3, 1.6
	3	2-Sep		I-V, KCL, KVL	1.4-1.6
2		5-Sep	Basic Inst.	UC Holiday (Labor Day)	
	4	7-Sep		Resistor Circuits, Node Analysis	2.1-2.4
	5	9-Sep		Node and Mesh Analysis (Resistors)	2.4-2.5
3	6	12-Sep	Scope	Thevenin, Norton, Superposition	2.6-2.8
	7	14-Sep		Dependent Sources in Circuits	2.4-2.5
	8	16-Sep		Equivalent Input/Output Circuit Blocks	2.6-2.8
4	9	19-Sep	Eq. Circuits	Capacitors and Inductors	3.1-3.7, light on 3.7
	10	21-Sep		RC Transients	4.1-4.2
	11	23-Sep		RL Transients and Logic as RC Circuit	4.3, VG
5	12	26-Sep	RC Trans.	Midterm #1 Definition; RC Model for Logic Gate Delay	VG Only
	13	28-Sep		Quiz; Cascade Delay and Dynamic Power	VG Only
	14	30-Sep		Midterm Review; Sinusoidal Source; Total Solution	4.4
6	15	3-Oct		Complex Number Manipulation and Phasors	5.1-5.2
		5-Oct		Midterm #1	
	16	7-Oct		Circuit Analysis with Phasors and Complex Impedances	5.3-5.4
7	17	10-Oct	Digital	Power and Equivalent Sources with Phasors	5.5-5.6
	18	12-Oct		Frequency Response	6.1-6.3
	19	14-Oct		Bode Plots, Resonance	6.4-6.7
8	20	17-Oct	Freq. Resp.	Op-Amps: Ideal	14.1-14.3
	21	19-Oct		Op-Amps: Design and Limtations	14.4-14.7
	22	21-Oct		Op-Amps: For Differentiation and Integration	14.8-14.10
9	23	24-Oct	Op-Amps	Diode: Physics and Load Line	10.1-10.2
	24	26-Oct		Diode: Circuit Model and Applications	10.4-10.5
	25	28-Oct		Diode: Circuits and Small-Signal Linearization	10.6-10.7;
10	26	31-Oct	Diode/MOS	Midterm #2 Definition; MOSFET: Physics	12.1; VG
	27	2-Nov		Quiz #2; MOSFET: I vs V and Load Line Solution	12.2-12.4
	28	4-Nov		MOSFET: NMOS and CMOS IV Models and Inverters	VG Only
11	29	7-Nov		CMOS Voltage Transfer Characteristics	VG Only
		9-Nov		Midterm #2	
		11-Nov		UC Holiday(Veterans Day)	
12	30	14-Nov	Project	Midterm Return, Lab Project, CMOS Issues	VG Only
	31	16-Nov		CMOS: Capacitance and Resistor Model for RC Delay	VG Only
	32	18-Nov		CMOS: Multipule Input Gates, Delays and Cascade	VG Only
13	33	21-Nov	Project	CMOS: Synchronization via Latches and Clocks	VG Only
	34	23-Nov		CMOS: Pipelining for Throughput at cost of Latency	VG Only
		25-Nov		UC Holiday (Thanksgiving)	
14	35	28-Nov	Project	Total Solution (Particular plus forced)	4.4
	36	30-Nov		RLC 2nd Order Response	4.5
	37	2-Dec		RLC 2nd Order Response (Cont.)	4.5
15	38	5-Dec	Project	Microfabrication	
	39	7-Dec		Nano Technology	
	40	9-Dec		Review	
Final		19-Dec		Final 8-11 AM	