EE 40 – Introduction to Microelectronic Circuits

Fall 2005,
Dept. EECS, 509 Cory
UC Berkeley
Course Web Site

Prof. A. R. Neureuther
neureuth@eecs.berkeley.edu, 642-4590
Office Hours: M1, W 3, F10
http://www-inst.eecs.berkeley.edu/~ee40/

Final Exam: December 19th, 2005

Closed Book, Closed Notes
Write on the Exam paper
Tear off Last Page with Device and 2nd Order Circuit Equations

Print Your Name:___Solution__ 12/19/05
Solutions for 'as given' and corrections shown.

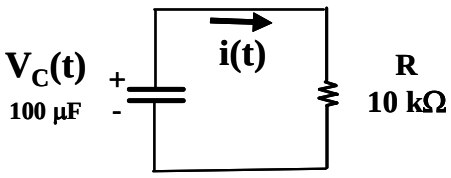
Sign Your Name:_____

Show your work so that the method as well as the answer can be graded for correctness and completeness. Correct answers alone are only worth 70% of full credit. Most of the points are for explicit evidence that you are taking a correct approach.

Problem	Possible	Score
I	50	
II	35	
III	45	
IV	30	
V	20	
VI	40	
Total	220	

I (50 Points) Transient

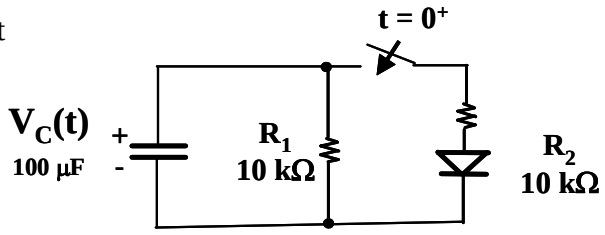
a) (15 Points) Find the current at t = 0.5 seconds.



$V_C(t=0) = 5V$

$$V_C(t) = A + Be^{-t/\tau}$$
$$A = 0$$
$$B = 5V$$
$$\tau = RC = 1s$$
$$i_C(t) = -C\frac{dV_C(t)}{dt} = -10^{-4}(-1/1s)5Ve^{-0.5/1}$$
$$= 500e^{-0.5/1}\mu A = 303\mu A$$

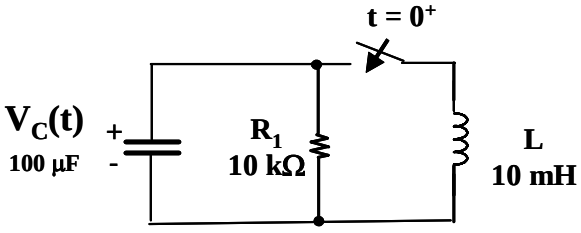
b) (15 Points) Assume that the switch closes at t = 0^+. Find an equation for the capacitor voltage versus time that is valid for a few hundred ms after the switch closes.



$V_C(t=0) = 5V$ **Use the large signal diode model**

$$V_C(t) = A + Be^{-t/\tau}$$
$$A = \frac{R_1}{R_1 + R_2}0.7V = 0.35V$$
$$B = 5V - A = 4.65V$$
$$\tau = (R_1 \parallel R_2)C = 0.5s$$
$$V_C(t) = 0.35V + 4.65Ve^{-t/0.5s}$$

c) (20 Points) Assume that the switch closes at t = 0^+. Give an algebraic expression for the capacitor voltage versus time that is valid for t > 0. Then give formulas for the parameters you use in terms of R, L and C and conditions for determining any unknowns. Do not solve.

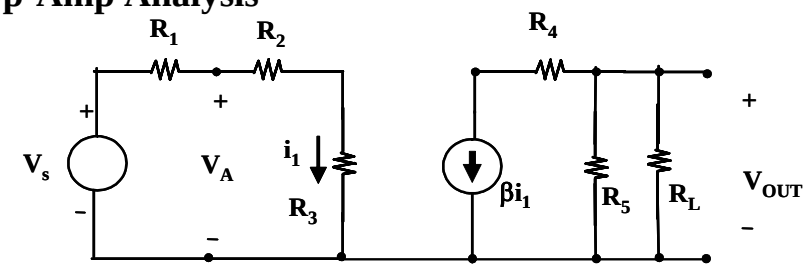


$V_C(t=0) = 5V$

$$\omega_0 = \frac{1}{\sqrt{LC}} = \frac{1}{\sqrt{10^{-2}10^{-4}}} = 1000$$
$$\alpha = \frac{1}{2RL} = \frac{1}{210^4 10^{-2}} = 0.005$$
$$\omega_n = \sqrt{\omega_0^2 - \alpha^2} \approx \omega_0 = 1000$$
$$V_C(t) = K_1 e^{-t\alpha}\cos(\omega_n) + K_2 e^{-t\alpha}\sin(\omega_n)$$
$$V_C(t=0) = K_1 = 5V$$
$$i_L(t=0) = 0 \Rightarrow -C\frac{dV_C(t)}{dt}_{t=0} = i_R(t=0)$$
$$-C\{-K_1\alpha + \omega_n K_2\} = \frac{5V}{10^4} = 500\mu A$$

II (35 Points) Circuit and Op-Amp Analysis

a) (15 Points) Find an algebraic expression for $\mathbf{V_{OUT}/V_A}$ for the circuit shown.

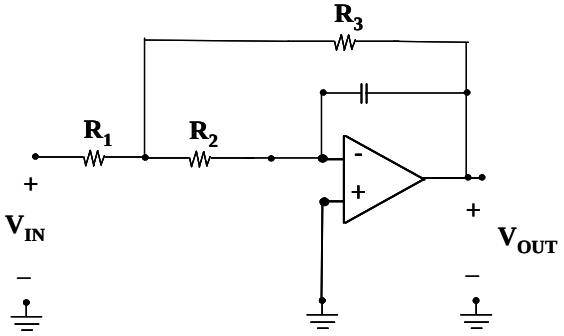


$$i_1 = \frac{R_3}{R_2 + R_3} V_A$$

$$V_{OUT} = -\beta i_1 \frac{R_L R_5}{R_L + R_5}$$

$$\frac{V_{OUT}}{V_A} = -\beta \frac{R_3}{R_2 + R_3} \frac{R_L R_5}{R_L + R_5}$$

b) (20 Points) Give a set of equations suitable for determining $\mathbf{V_{OUT}/V_{IN}}$ for the Op-Amp circuit below. Do not solve but outline the solution procedure. That is give the number of unknowns, the number of equations, which is solved for what and substituted into what, etc.



$$Add\_Node\_V_B\_Between\_R_1\_and\_R_2$$

$$\frac{V_B}{R_2} + C\frac{dV_0}{dt} = 0$$

$$\frac{V_B}{R_2} + j\omega C V_0 = 0$$

$$\frac{V_{IN} - V_B}{R_1} + \frac{0 - V_B}{R_2} + \frac{V_{OUT} - V_B}{R_3} = 0$$

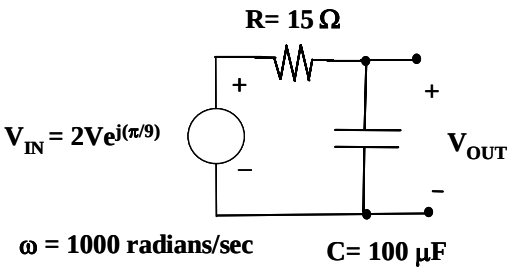
$$Solve\_2nd\_eq\_for\_V_B$$

$$Sub\_in\_to\_3rd\_eq$$

$$Solve\_3rd\_eq\_for\_V_{OUT}$$

III (45 Points) Phasors and Bode Plots

a) (20 Points) Find $V_C(t = 0)$ in the circuit.



$$\mathbf{V}_C = \frac{Z_C}{R + Z_C}\mathbf{V}_{IN} = \frac{(1/\,j\omega C)}{R + (1/\,j\omega C)}\mathbf{V}_{IN}$$

$$\mathbf{V}_C = \frac{(1/\,j\omega C)}{R + (1/\,j\omega C)}\mathbf{V}_{IN}$$

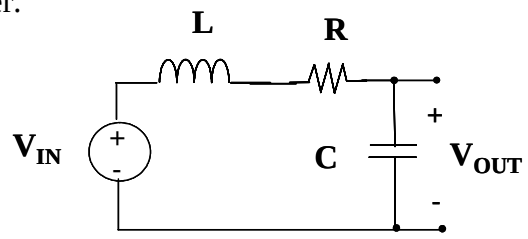
$$\mathbf{V}_C = \frac{(-j10)}{15 - j10}2\angle 20^o$$

$$\mathbf{V}_C = \frac{10\angle -90^o}{18.03\angle -33.9^o}2\angle 20^o$$

$$\mathbf{V}_C = 1.11\angle -36.3^o$$

$$\mathbf{V}_C(t = 0) = 1.11\cos(-36.3) = 1.11 \cdot 0.806 = 0.89V$$

b) (16 Points) Find the asymptotic behavior of V_{OUT}/V_{IN} the circuit below as ω goes to zero and infinity. The asympototic behavior is $Ae^{j\phi}\omega^n$ where A is the magnitude, ϕ is the phase in radians and n is a positive or negative integer.



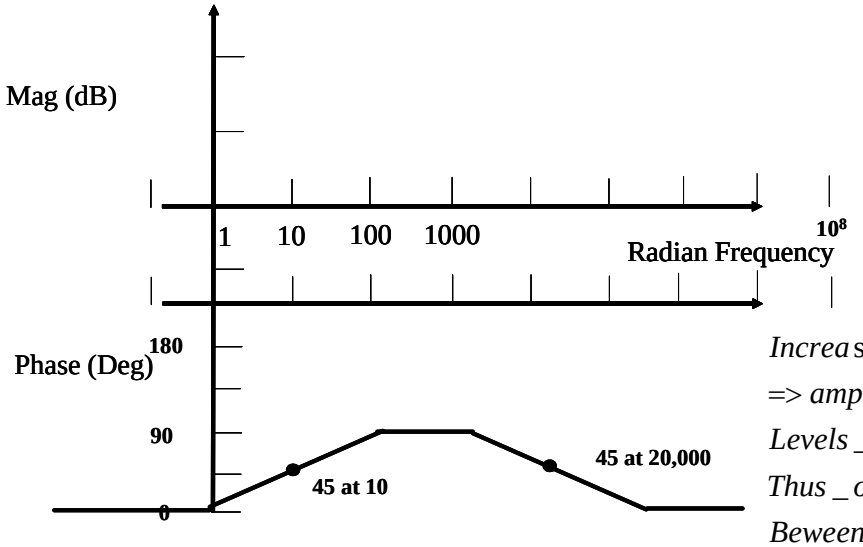
$$\mathbf{V}_{OUT} = \frac{Z_C}{Z_L + R + Z_C}\mathbf{V}_{IN} = \frac{(1/\,j\omega C)}{j\omega L + R + (1/\,j\omega C)}\mathbf{V}_{IN}$$

$$\frac{\mathbf{V}_{OUT}}{\mathbf{V}_{IN}} = \frac{1}{1 + j\omega CR - \omega^2 LC}$$

$$\omega \to 0 \Rightarrow 1\angle 0^o\,\omega^0$$

$$\omega \to \infty \Rightarrow \frac{1}{-\omega^2 LC} \Rightarrow \frac{1}{LC}\angle 180^o\,\omega^{-2}$$

c) (9 Points) Given that the low frequency gain of a circuit is constant at an amplitude of 4 determine the gain at $\omega = 10^8$ from only the phase of the Bode plot.

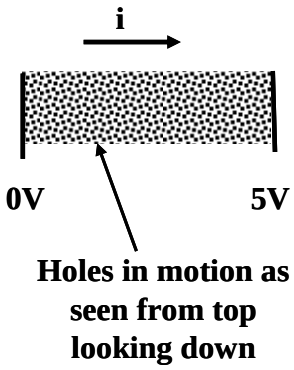


$Increa\sin g\_Phase \Rightarrow Factor\_in\_numerator$
$\Rightarrow amplitude\_increa\sin g$
$Levels\_off\_when\_phase\_decreases$
$Thus\_only\_increases\_by\_amount$
$Beween\_the\_45\_deg ree\_po\int s$

$$Gain = 4\frac{\omega_2}{\omega_1} = 4\frac{20000}{10} = 8000$$

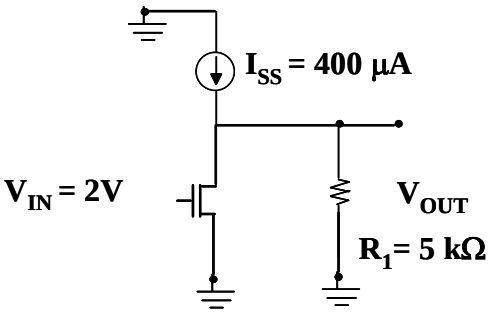
IV (30 Points) Devices

a) (15 Points) A 1 μm wide by 5 μm long p-type strip of silicon of unknown thickness produces 100 μA of current when a voltage of 5 volts is applied from end to end across the length of the strip. Estimate the number of holes per unit area in the top down layout view required to produce this current. Assume the p-type doping is 10^{15} /cm^3.



$$All\_moving\_charge\_regardless\_of\_depth$$
$$contributes\_to\_the\_current$$
$$i = Q_{per\_cm^2} \cdot velocity \cdot width$$
$$velocity = \mu_p E = \mu_p \frac{5V}{5\mu}$$
$$From\_Chart\_\mu_p = 480\frac{cm^2}{Vs}$$
$$N_{per\_cm^2} = \frac{Q_{per\_cm^2}}{q} = \frac{i}{q\mu_p E \cdot width}$$
$$N_{per\_cm^2} = \frac{100\mu A}{1.6\cdot 10^{-19} \bullet 480\frac{cm^2}{Vs} 10^4 \frac{V}{cm} \bullet 10^{-4} cm}$$
$$N_{per\_cm^2} = 1.3\cdot 10^{12}\frac{holes}{cm^2}$$

b) (15 Points) Use a graphical method to determine the drain current and drain to source voltage for the circuit shown. Use the long channel device model.

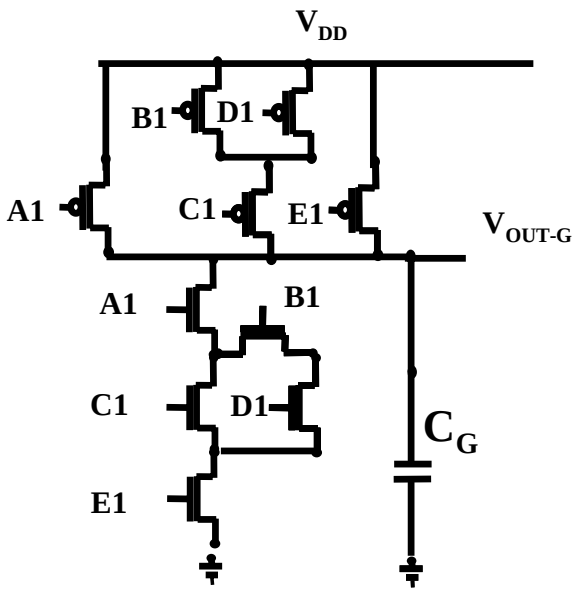


$$Use\_Thevenin$$
$$V_{OC} = 400\mu A \cdot 5000\Omega = 2V$$
$$I_{SC} = 400\mu A$$
$$Use\_Graph\_for\_regular$$
$$(and\_not\_velovity\_saturated)$$
$$V_{GATE} = 2V\_curve$$
$$I_D = 290\mu A$$
$$V_D = 0.7V$$

$$With\_40\mu A\_Source$$
$$Use\_Thevenin$$
$$V_{OC} = 40\mu A \cdot 5000\Omega = 0.2V$$
$$I_{SC} = 40\mu A$$
$$Use\_Graph\_for\_regular$$
$$(and\_not\_velovity\_saturated)$$
$$V_{GATE} = 2V\_curve$$
$$I_D = 30\mu A$$
$$V_D = 0.05V$$

V (20 Points) CMOS Gates

Determine the overall best case delay and overall worst case delay relative to an inverter for the circuit show. For the best and worst case delays give an example of a set of initial input values and then the changes in the input values that will result in the delay .



$Slowest\_is\_H\_to\_L$

$Through\_A1\_B1\_D1\_E1 => 4\tau_{INVERTER}$

$Fastest\_is\_L\_to\_H$

$Through\_1\_1\_and 1.5\_in\_parallel$

$Fastest\_is\_\frac{1}{2}||\frac{1}{1.5}=\frac{3}{8}\tau_{INVERTER}$

$Example\_Create\_Slowest$

$A1=B1=E1=1\_with\_C1=D1=0$

$then\_D1=>1$

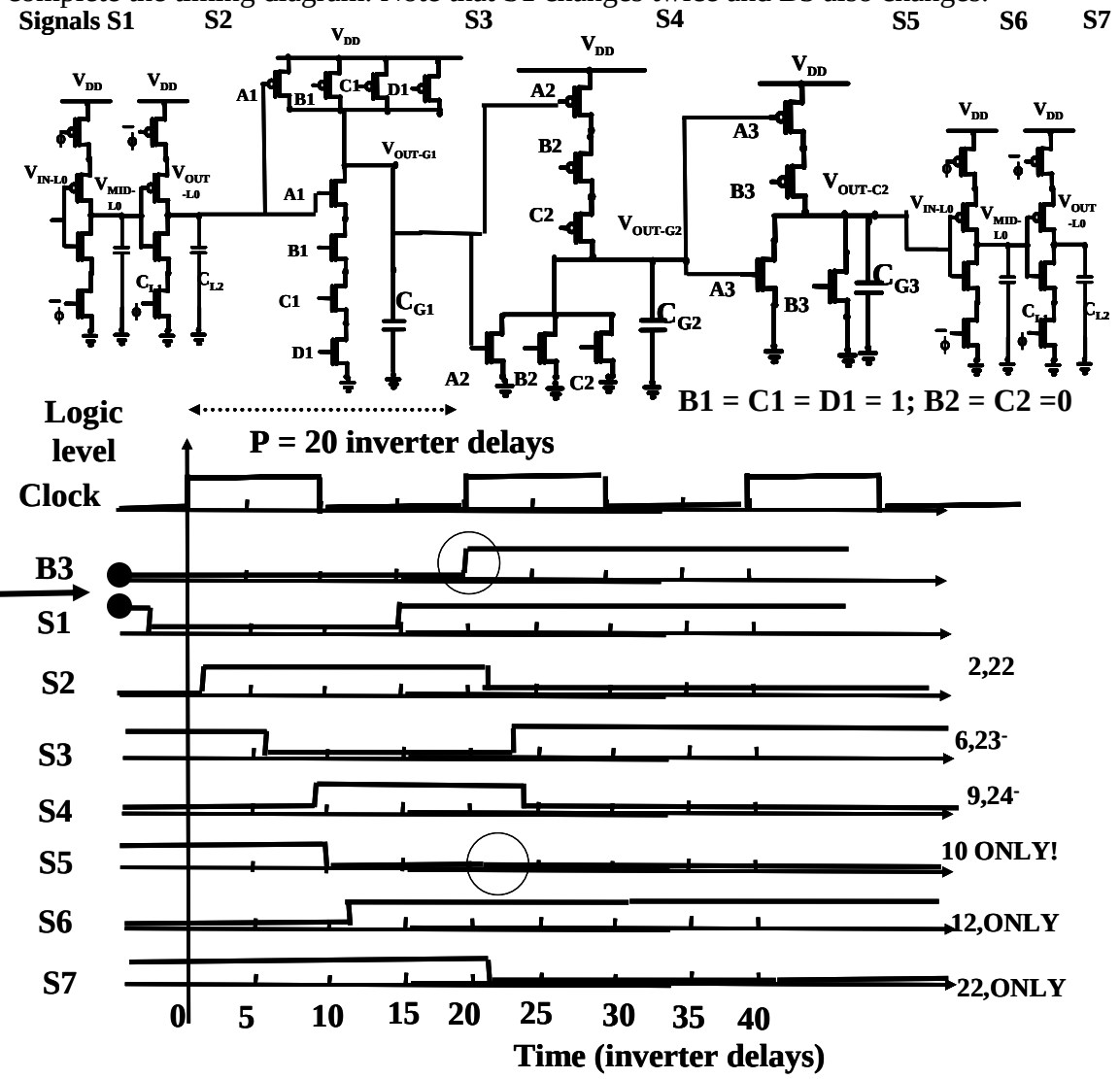
$Example\_Create\_Fastest$

$A1=C1=E1=1\_with\_B1=D1=0$

$Then\_A1=C1=E1=>0$

VI (40 Points) Gates and Latches

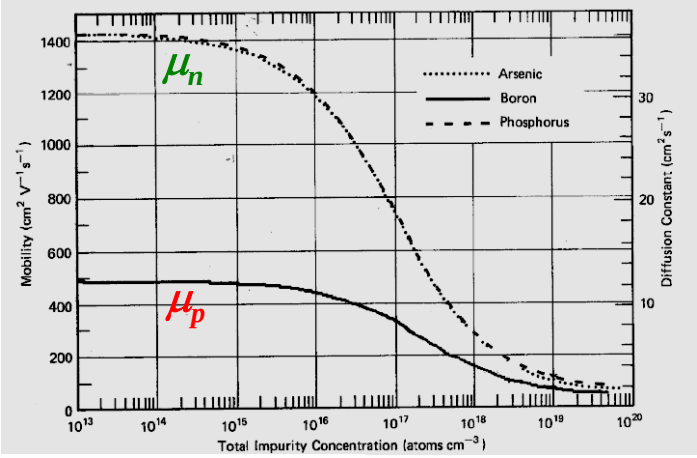
a) (22 Points) Assuming that the initial inputs have been present for several clock cycles, complete the timing diagram. Note that S1 changes twice and B3 also changes.

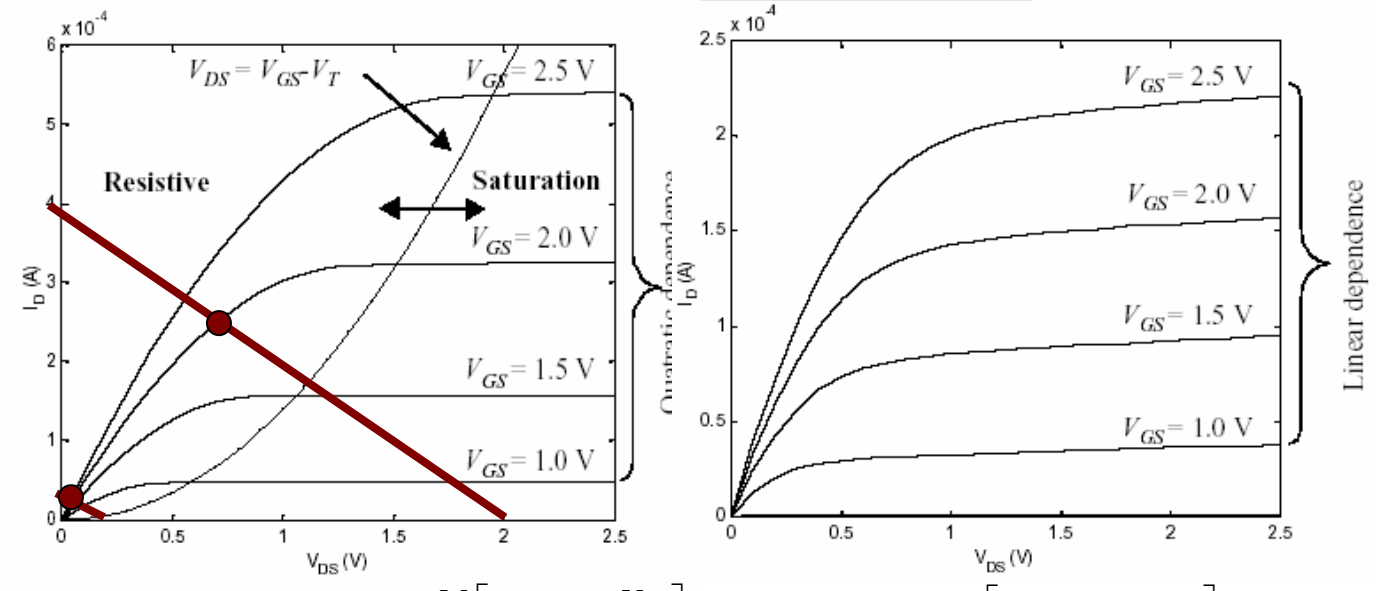


b) (18 Points) Several pipeline designs are possible. Find the one that reduces the product of the clock period times the latency. In computing the clock period and the latency assume that there is one-half of the double CMOS latch on each end of the logic. Hint: Start by finding the minimum clock period for the lumped implementation above.

Assuming that G3 could be either a 2-input NAND or a 2-input NOR the delay in G3 is 2τ: As lumped cock Period would need to be 4+3+2+2+2 =13; Latency would be 13; Product =169. If divide in to two stages where first stage is G1 and second stage is G2+G3, then G2+G3 sets clock high to 3+2+2 = 7 and low of 2 gives clock period of 9. Latency becomes 18 and Product becomes 162 **which is lower**. Going to three stages would give P = 4+2+2=8; Latency = 3 x 8 =24 and Product = 192. Putting G1 and G3 together gives clock high of 4+3+2+2 = 11 and period of 13. Latency is 26 and Product is 338.

Device and 2nd Order Transient Equations





$$I_D = k_n' \frac{W}{L}\left[V_{GS} - V_T - \frac{V_{DS}}{2}\right]V_{DS} \qquad I_{DSAT} = WC_{ox}\left[V_{GS} - V_T - \frac{V_{DSAT}}{2}\right]v_{sat}$$

where $k_n' = \mu_n C_{ox}$ where $V_{DSAT} = \frac{L}{\mu_n} v_{sat}$

$$\alpha = \frac{R}{2L} SeriesCircuit$$

$$\alpha = \frac{1}{2RL} ParallelCircuit$$

$$\omega_0 = \frac{1}{\sqrt{LC}}$$

$$\frac{d^2 i(t)}{dt^2} + 2\alpha \frac{di(t)}{dt} + \omega_0^2 i(t) = 0$$

$$s^2 + 2\alpha s + \omega_0^2 = 0$$

$$s_1 = -\alpha + \sqrt{\alpha^2 - \omega_0^2}$$

$$s_2 = -\alpha - \sqrt{\alpha^2 - \omega_0^2}$$

$$i_{Char}(t) = K_1 e^{s_1 t} + K_2 e^{s_2 t}$$

$$i_{Char}(t) = K_1 e^{s_1 t} + K_2 t e^{s_1 t}$$

$$i_{Char}(t) = K_1 e^{-\alpha t}\cos(\omega_n t) + K_2 e^{-\alpha t}\sin(\omega_n t)$$

$$\omega_n = \sqrt{\omega_0^2 - \alpha^2}$$