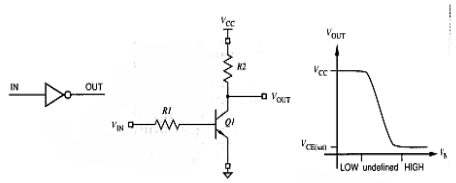
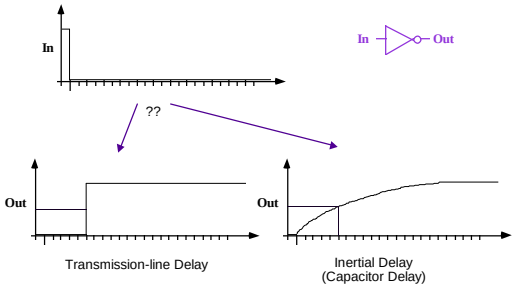
Outline

- Last time:
  - Design versus Implementation
  - Specification, Description, and Depiction
  - Conceptual Blocks & How to Overcome Them
  - Good Versus Bad Design
  - The Role of Language in Design
  - The CS150 Project
- This lecture:
  - Introduction to timing diagrams
  - SR latch
  - D latch
  - Flip-Flops
  - Shift Registers
  - Serial-Parallel Conversion

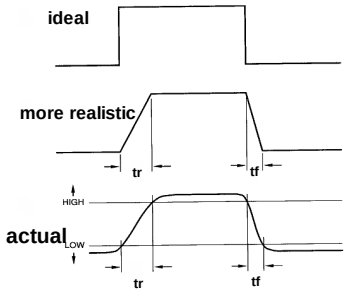
Resistor-Transistor Inverter



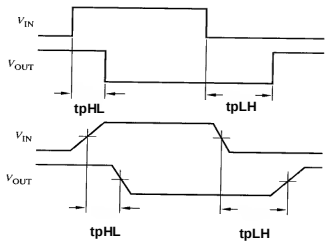
Inertial & Transmission-Line Delays



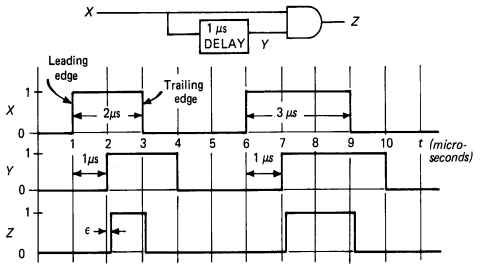
Transition Times



Propagation Delay



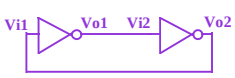
Timing Diagrams



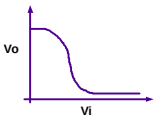
Latches and Flip-Flops

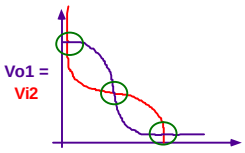
- Basic building-blocks of most sequential circuits
- Usual terminology:
  - *Flip-flop:* samples its inputs and changes its outputs at times determined by a "clocking signal."
  - *Latch:* Watches all of its inputs continuously and may change its outputs at any time.

Feedback in Digital Circuits

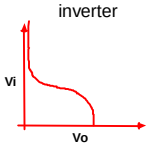


Vi2 = Vo1 = 0 1
Vi1 = Vo2 = 1 0

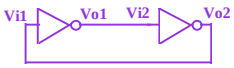




inverter



Feedback in Digital Circuits



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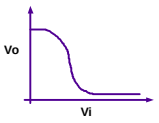
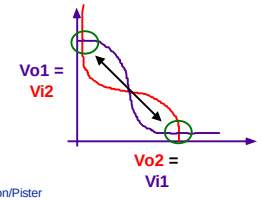
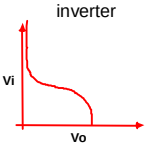
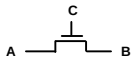




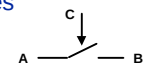
inverter



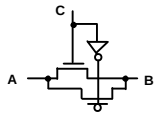
Implementation of Logic Using Switches



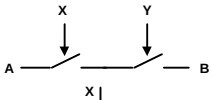
NMOS

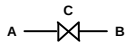


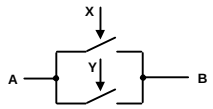
Switch, Relay



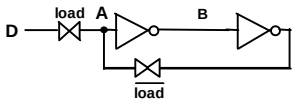
CMOS





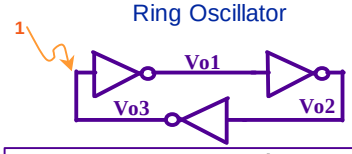


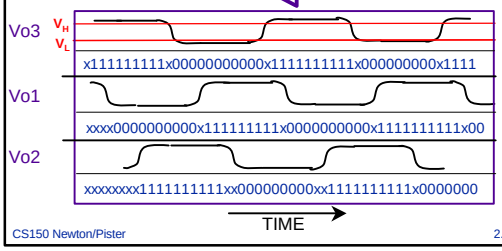
Setting the Values We Want



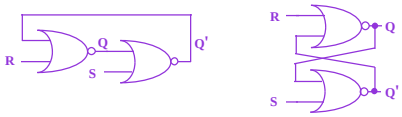
Data Latch
D-Latch

Ring Oscillator



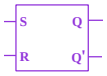


The Set-Reset (SR, RS) Latch

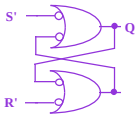


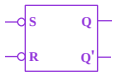
Latch Behavior

S	R	Q	Q'
0	0	last Q	last Q'
0	1	0	1
0	0	1	0
0	1	0	0



The S'-R' Latch

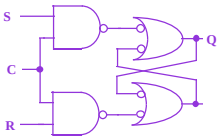


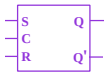


Latch Behavior

S'	R'	Q	Q'
0	0	0	0
0	1	1	0
1	0	0	1
1	1	last Q	last Q'

S-R Latch With Enable

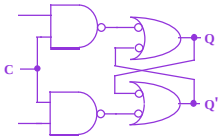




Latch Behavior

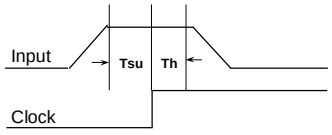
S	R	C	Q	Q'
0	0	1	last Q	last Q'
0	1	1	0	1
1	0	1	1	0
1	1	1	1	1
*	*	0	last Q	last Q'

Data (D) Latch

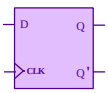


Setup and Hold Times for Latches

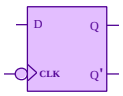
- **Setup Time (Tsu)** is the minimum time interval for which the input signal must be stable (unchanging) *prior to* the sampling event of the clock for the input signal to be recognized correctly.
- **Hold Time (Th)** is the minimum time interval for which the input signal must be stable (unchanging) *following* the sampling event of the clock for the input signal to be recognized correctly.



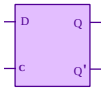
Standard Latch & Flip-Flop Conventions



Positive-Edge-Triggered D Flip-flop



Negative-Edge-Triggered D Flip-flop



D Latch with Enable

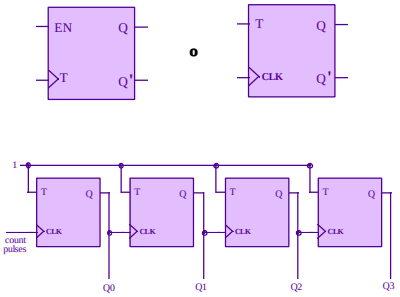
Input/Output Behavior of Latches and Flip-Flops

Type	When Inputs Sampled	When Outputs Valid	Tsu, Th Relative to:
Unclocked Latch	always	Tprop from input change	–
Level-Sensitive Latch	clock high	Tprop from input change	Falling clock edge
Positive edge triggered flip-flop	clock low → high transition	Tprop from rising clock edge	Rising clock edge
Negative edge triggered flip-flop	clock high → low transition	Tprop from falling clock edge	Falling clock edge
Master-slave flip-flop	clock high → low transition	Tprop from falling clock edge	Falling clock edge

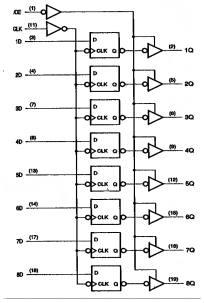
Latch & Flip-Flop Characteristic Equations

S-R Latch	Qn+1 = S + R'Qn
D latch	Qn+1 = D
✲ Edge-triggered D Flip-Flop	Qn+1 = D
Master-slave S-R Flip-Flop	Qn+1 = S + R'Qn
Master-Slave J-K Flip-Flop	Qn+1 = JQn' + K'Qn
Edge-Triggered J-K Flip-Flop	Qn+1 = JQn' + K'Qn
✲ T Flip-Flop	Qn+1 = Qn'
✲ T Flip-Flop with Enable	Qn+1 = EQn' + E'Qn = E ⊕ Qn

Toggle (T) Flip-Flop

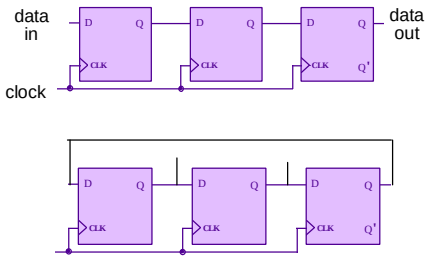


Registers

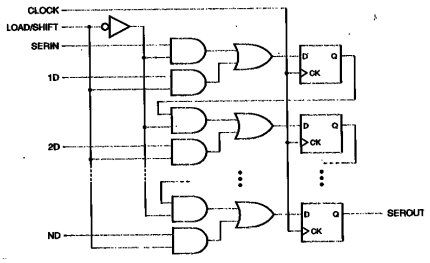


- *Tri-state Outputs*: Output can be logic-0, logic-1, or "high impedence" (off, disconnected). Very important for connections to a "bus".

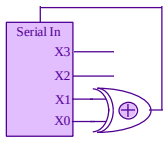
Shift Registers & Ring Counters



Parallel/Serial Shift Register



Linear Feedback Shift Registers (LFSR)



n	Feedback equation
2	X2 = X1 ⊕ X0
3	X3 = X1 ⊕ X0
4	X4 = X1 ⊕ X0
5	X5 = X2 ⊕ X0
6	X6 = X1 ⊕ X0
7	X7 = X3 ⊕ X0
8	X8 = X4 ⊕ X3 ⊕ X2 ⊕ X0
12	X12 = X6 ⊕ X4 ⊕ X1 ⊕ X0
16	X16 = X5 ⊕ X4 ⊕ X3 ⊕ X0
20	X20 = X3 ⊕ X0
24	X24 = X7 ⊕ X2 ⊕ X1 ⊕ X0
28	X28 = X3 ⊕ X0
32	X32 = X22 ⊕ X2 ⊕ X1 ⊕ X0