Additional space for Working Problems

Your Name: ______________________________________

(4) Derive a **block diagram for a bit-serial sequential circuit** that can be used for **computing the odd-parity for a 32-bit, bit-serial number**, A<31:0>, **represented in sign-magnitude form**, where bit 31 (the last bit to arrive) is the sign bit. Describe how your circuit operates.

4. (10pts)

Additional space for Problem 4

(c) **Obtain a circuit diagram for an implementation of the machine.** Use the **minimum number of logic gates (AND, OR, NAND, NOR, XOR, XNOR, or inverters)** and **positive-edge-triggered T flip-flops only.**

3(c) (10pts)

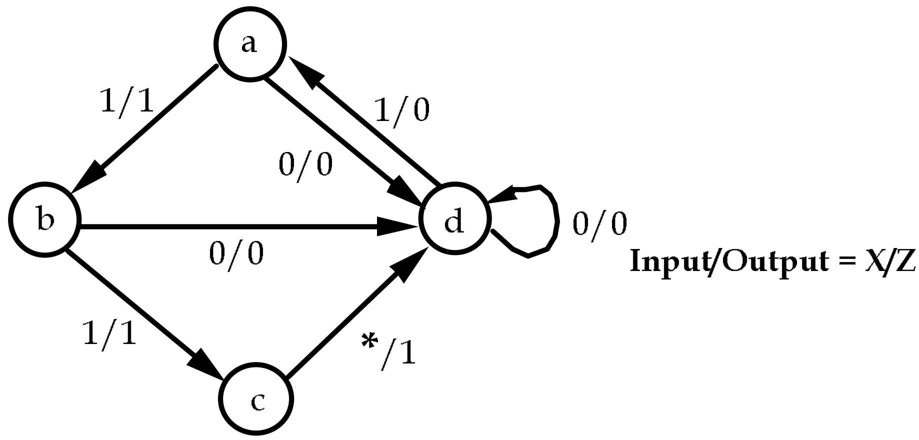
(c) **Using your next-state table from Part 3(a)** above, **construct an implication table** and check for state equivalence. **List the equivalent states. Enter the word NONE below if you cannot find any equivalent states from your table.**

3(d) (6pts)

Equivalent States: ______________

Your Name: ____

(3) Consider the following state-transition graph which is to be **implemented as a clocked, synchronous sequential circuit.**



(a) Construct a **state transition table** for the machine in terms of **input** X and **present-state (PS)** for **output** Z and **next-state (NS).**

3(a) (4pts)

(b) **Assume the states are encoded a=00, b=01, c=11, and d=10. Use Karnaugh map(s)** to obtain the **reduced next-state and output equations** for the machine. **Show your Karnaugh map(s.)**

3(b) (10pts)

Additional space for Problem 2

Your Name: ____

(2) For the following state table, where X_1 and X_2 are inputs and Z_1 and Z_2 are outputs:

PS	$X_1X_2 = 00$		$X_1X_2 = 01$		$X_1X_2 = 10$		$X_1X_2 = 11$	
	NS	Z_1Z_2	NS	Z_1Z_2	NS	Z_1Z_2	NS	Z_1Z_2
A	A	00	C	00	B	00	D	00
B	B	00	B	00	D	10	D	10
C	C	01	A	01	C	01	A	01
D	B	01	B	01	C	10	A	10

(a) Use the **three guidelines for state assignment** to determine **which of the three possible non-equivalent state assignments should result in the best implementation**. Show all steps and explain your choice. **Do *not* attempt to reduce the state table first.**

(b) Using your answer to (a) above, **derive T flip-flop input equations and the output equations**. All equations stated should contain a **minimum number of literals**. Show all steps.

2(a) (10pts) State codes:

A = ____ **B =** ____ **C =** ____ **D =** ____

2(b) (20pts) Equations:

T1 = ____

T2 = ____

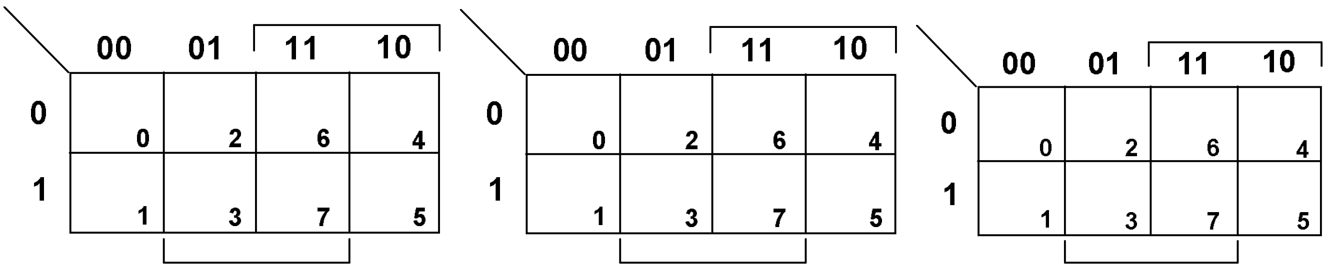
Z1 = ____

Z2 = ____

(ii) Draw **Karnaugh maps for each output** and use them to simplify the functions.

(iii) Draw a **schematic diagram** using the **minimum number of NAND gates and inverters only**. The NAND gates may have any number of inputs.

1(b) (9pts) (ii) Karnaugh Maps:



(iii) (9pts) Schematic diagram:

Additional space for Problem1

Your Name: ____

(1)	/30
(2)	/30
(3)	/30
(4)	/10
TOTAL	/100

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Department of Electrical Engineering
and Computer Sciences

CS 150 - Spring 1995
Prof. A. R. Newton

Quiz 2

Room 10 Evans Hall, 2:10pm Tuesday April 4
(Open Katz only, Calculators OK, 1hr 20mins)

Include all final answers in locations indicated on these pages. Use space provided for all working. If necessary, attach additional sheets by staple at the end. BE SURE TO WRITE YOUR NAME ON EVERY SHEET.

(1) (a) Using **exactly 5 bits**, express the following numbers in **2's-complement form:**

1(a) (6pts) **(i) 7** = __ __ __ __ __
(ii) -11 = __ __ __ __ __
(iii) 31 = __ __ __ __ __

(b) Design a circuit to compute the **two's complement** of a **3-bit binary number**. The inputs are b_0, b_1 and b_2, where b_2 is the most significant digit and the outputs are c_0, c_1 and c_2 where c_2 is the most significant digit.

(i) Show a **truth table** for the circuit.

1(b) (i) (6pts) Truth table: