Additional space for Problem 3

Your Name: ____

(g) Modify your combinational logic, if necessary, to **eliminate hazards** from the design. State what you are doing and why you are doing it. (2pts)

(h) Draw a **gate-level asynchronous sequential circuit diagram** for the design. Represent the asynchronous delay element(s) in feedback loops with a buffer symbol. (4pts)

(e) Examine the reduced flow table and **add additional states if necessary to obtain a critical-race-free state assignment** for the circuit. (hint: requires two state bits) (3pts)

(f) Construct a composite **Karnaugh map for the next-state and external output logic functions** from your state assignment. (3pts)

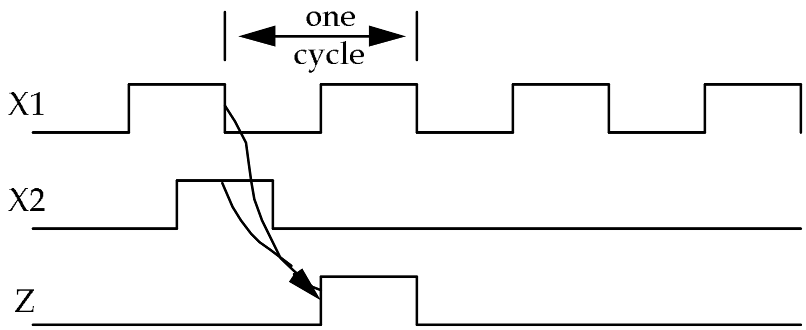
Your Name: ______________________________________

(b) Use an **implication table** to find all possible pairs of equivalent or compatible states (3pts).

(c) Construct a **merger diagram** from the results of (b) and **list the sets of mergeable states that will lead to the minimum number of states** for the design. (3pts)

(d) Obtain a **reduced flow table** from the above, giving a **unique state name to each group of states merged** into a single state (hint: I ended up with 3 merged states, in Moore form). (3pts)

(3) Design a fundamental mode asynchronous circuit with two inputs and one output. Input X1 is driven by the system clock. Input X2 is an asynchronous input. If X2 is logic 1 when X1 changes from 1 to 0, then output Z follows the waveform of input X1 for one cycle (i.e. until X1 changes again from 1 to 0.) If X2 is a logic 0 when X1 changes from 1 to 0, then Z is a logic 0 until X1 changes again from 1 to 0. Example behavior is shown in the timing diagram below. The circuit should be designed so that it is logic hazard-free, has a race-free state assignment, and can recover from illegal or unused states.

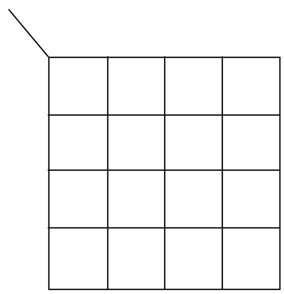


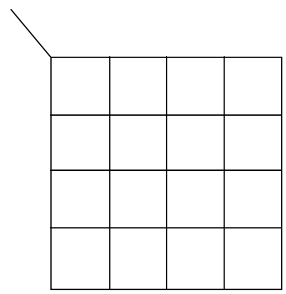
(a) Use the word description and timing diagram above to obtain a **primitive flow table** for the problem (hint: I used 7 symbolic states in Moore form) (4pts)

(e) Show a **schematic diagram** for the bus arbiter using **positive edge-triggered JK flop flops.** (3pts)

Extra space for Problem 2

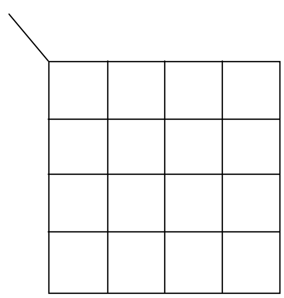
(c) If the idle state is encoded as Y1 Y2 = 0 0, State A is encoded as Y1 Y2 = 0 1 and State B as Y1 Y2 = 1 1, derive the **Karnaugh maps for the next-state and output functions.** (4pts)

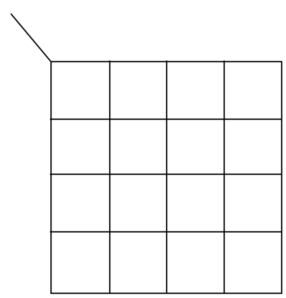




Y1' Y2' **OA OB**

(d) If the machine is to be implemented using **JK flip-flops**, obtain the **Karnaugh maps for the JK flip-flop excitation inputs**. Write the **excitation input and external output equations** for the design. (10pts)





J1 J2 **K1 K2**

J1 = ______________________________

J2 = ______________________________

K1 = ______________________________

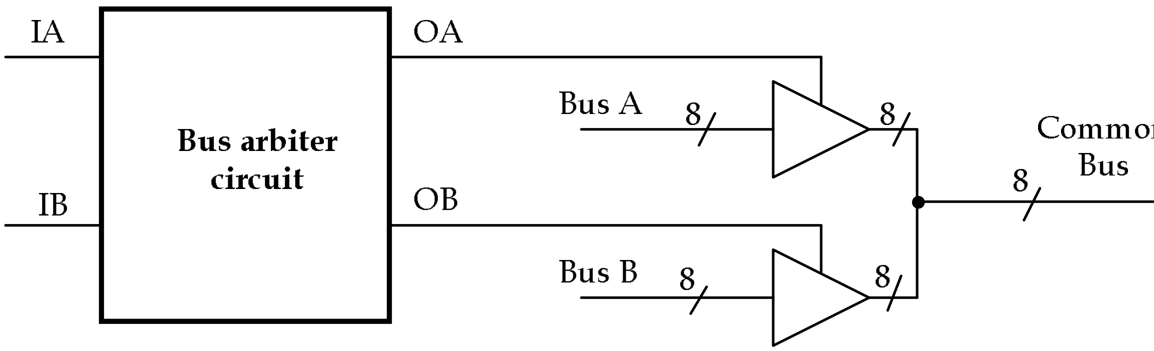
K2 = ______________________________

OA= ______________________________

OB = ______________________________

Your Name: ____

(2) You are to design a bus arbiter that operates as follows. When inputs IA IB = 0 0 the circuit either goes into the idle state (outputs OA OB = 0 0, disabling both Bus A and Bus B buffers), or remains in the idle state. When inputs IA IB change to 1 0 or 1 1 the circuit goes into State A (outputs OA OB = 1 0 enabling the Bus A buffers and disabling the Bus B buffers.) When inputs IA IB change to 0 1 while in the idle state, the circuit goes to State B (outputs OA OB = 0 1 disabling Bus A buffers and enabling Bus B buffers.) To go from State A to State B requires input IA IB = 01, and to go from State B to State A requires inputs IA IB = 1 0.



(a) Construct a **State Transition Graph** for the bus arbiter in **Moore form.** (5pts)

(b) Derive a **State Transition Table** from your graph, also in Moore form. (3pts)

(c) Draw a **state transition graph (STG)** for the machine **showing all possible states and all possible transitions** (7pts)

(d) **Does the machine contain any redundant states?** If so, which state(s) are redundant and how can they be removed? **Draw an irredundant STG for the machine.** (7pts)

Your Name: ____________________________________

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Department of Electrical Engineering
and Computer Sciences

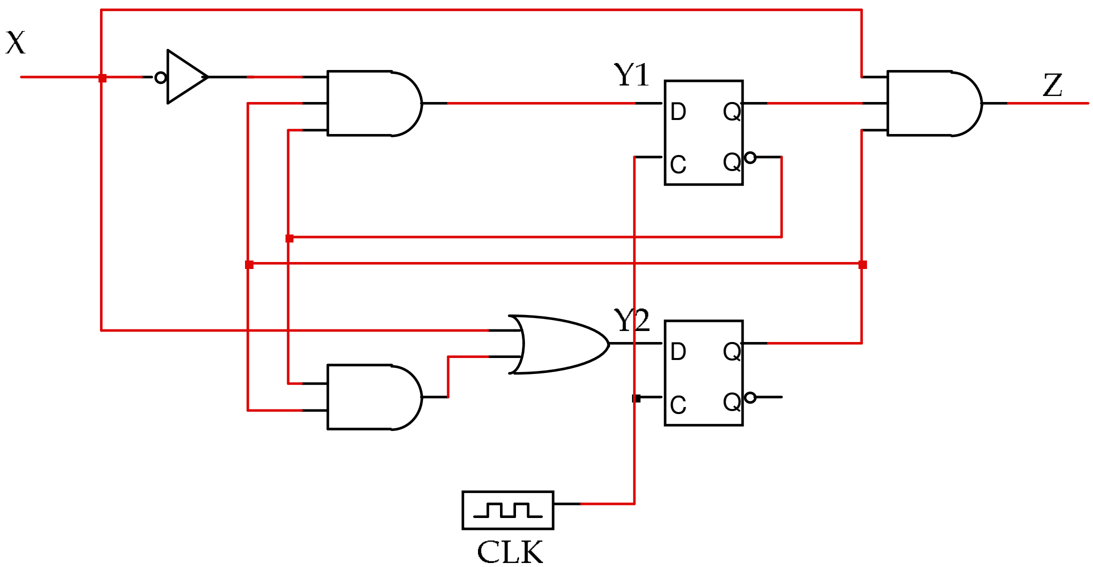
CS 150 - Spring 1994
Prof. A. R. Newton

Quiz 2

Room 145 Dwinelle, Tuesday 4/5
(Open Katz, Calculators OK, 1hr 20min)

Include all final answers in locations indicated on these pages. Use reverse side of sheets for all working. If necessary, attach additional sheets by staple at the end. BE SURE TO WRITE YOUR NAME ON EVERY SHEET.

(1) Consider the logic schematic diagram shown below:



(a) Is this a **Moore or Mealy** machine? ________________ (2pts)

(b) What are the **next-state** and **output equations** for this machine? (9pts)

(i) Y1 = ____________________________________

(ii) Y2 = ____________________________________

(iii) Z = ____________________________________