Guideline 1: _{S0,S1,S3,S5}, {S3,S5}, {S4,S6}, {S0,S2,S4,S6}___

Guideline 2: __{S1,S2}, {S2,S3}, {S1,S4}, {S2,S5}x2, {S1,S6}x2_

Guideline 3: __{S0,S1,S2,S3,S4,S6}, {S0,S1,S2,S3,S4,S5}__

(ii) (3 pts) Karnaugh Map for Assignment:

A \ BC	00	01	11	10
0	S0$_{0}$	S2$_{2}$	S4$_{6}$	S6$_{4}$
1	$_{1}$	S5$_{3}$	S3$_{7}$	S1$_{5}$

or

A \ BC	00	01	11	10
0	S0$_{0}$	S1$_{2}$	S3$_{6}$	S5$_{4}$
1	$_{1}$	S6$_{3}$	S4$_{7}$	S2$_{5}$

(iii) (3 pts) Final State Assignment:

S_0 = _000_ S_1 = _110_ S_2 = _001_

S_3 = _111_ S_4 = _011_ S_5 = _101_ S_6 = _010_

(iv) (3 pts) Constraints not satisfied:

___{s0,s1,s3,s5}, {s1,s2}, {s2,s3}, {s1,s4}___________

___all output constraints________________________

3(c) (6pts) ROM size:

Number of address lines: __4__

Number of data bits at each address: __3 or 4__

Total number of ROM bits: __(2^4)4 = 64 or (2^4)3 = 48__

(3) Consider the state table for a Mealy machine shown below:

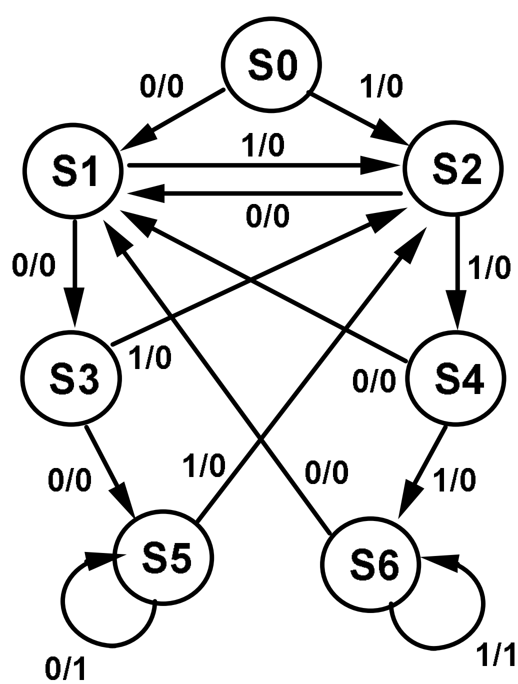
	next state		output Z	
	x=0	x=1	x=0	x=1
S_0	S_1	S_2	0	0
S_1	S_3	S_2	0	0
S_2	S_1	S_4	0	0
S_3	S_5	S_2	0	0
S_4	S_1	S_6	0	0
S_5	S_5	S_2	1	0
S_6	S_1	S_6	0	1

(a) Draw a **state transition graph** for the machine showing all input/output transitions and symbolic states.

(b) Use the **guidelines presented in class for state assignment** to select an optimal state assignment (for minimum logic). **Show all constraints**, your **final state assignment**, and indicate **which constraints are not satisfied by the assignment**.

(c) If a **ROM where used to implement the next-state and output logic** for a **D-flip-flop-based implementation** of your machine, how big would it have to be?

3(a) (4 pts) State Transition Graph:



3(b) (i) (6 pts) Constraints:

2(c) (i) (2pts) Karnaugh Maps:

R \ Q1Q0	00	01	11	10
0	1 (0)	(2)	1 (6)	(4)
1	(1)	1 (3)	(7)	1 (5)

D1

R \ Q1Q0	00	01	11	10
0	1 (0)	(2)	(6)	1 (4)
1	1 (1)	(3)	(7)	1 (5)

D0

(ii) (6pts) Flip-flop Input Equations & clock generation:

_D1 = (Q1 xor Q0 xor R)'________________________

_D0 = Q0'_______________________________________

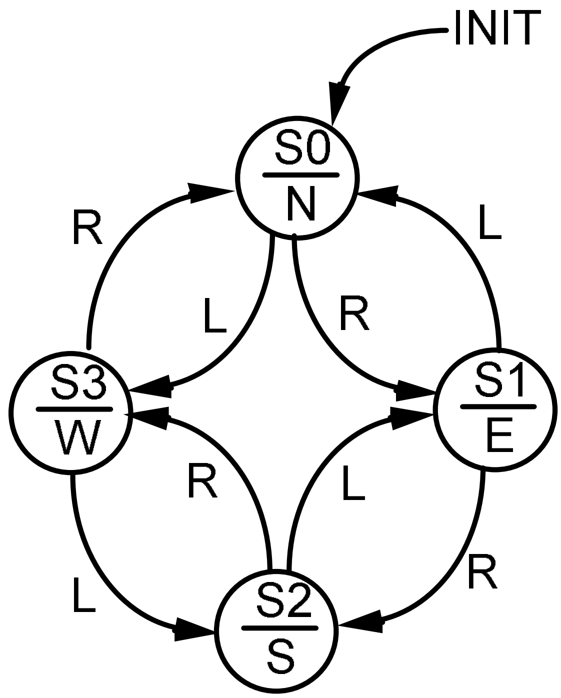
CLK = __L + R___________

(iii) (4pts) Output Equations:

N = _____Q0'Q1'_______   E = _____Q1'Q0_________

S = ______Q1Q0'_______   W = _____Q1Q0_________

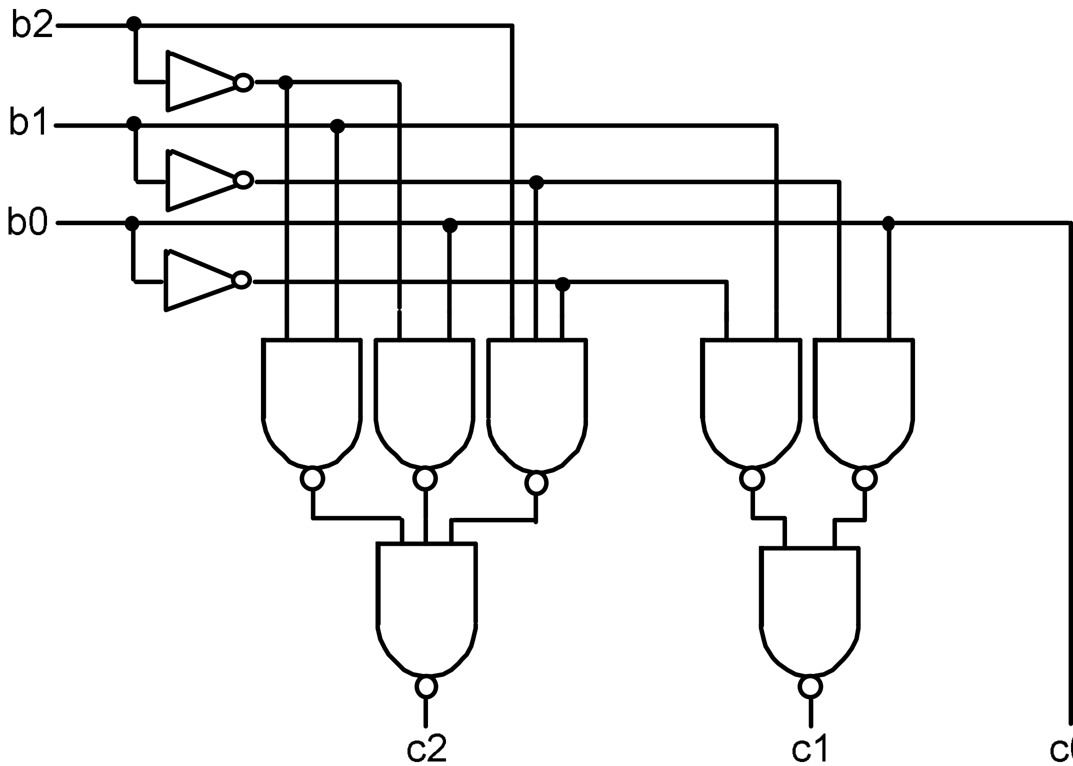
(iv) (7pts) Schematic Diagram:



2(b) (2pts) State Table:

	Input		P.S.		N.S.		Output			
	L	R	Q1	Q0	D1	D0	N	E	S	W
N	0	1	0	0	0	1	0	1	0	0
N	1	0	0	0	1	1	0	0	0	1
E	0	1	0	1	1	0	0	0	1	0
E	1	0	0	1	0	0	1	0	0	0
S	0	1	1	0	1	1	0	0	0	1
S	1	0	1	0	0	1	0	1	0	0
W	0	1	1	1	0	0	1	0	0	0
W	1	0	1	1	1	0	0	0	1	0

(iii) Schematic diagram:



(2) You are to design a "Manhattan Compass" which is an automobile accessory which has four display lights labelled North, South, East, and (yes, you guessed it...) West. One of the lights is always lit and indicates which direction the car is facing. There are two sensors on the steering wheel, labelled Right and Left. The wires connected to each of the right and left sensors has the value 1 when the position of the steering wheel is to the right or left of center respectively and a value of 0 otherwise. In addition, there is a button labelled INIT which, when pushed, tells the system that the car is stationary, the steering wheel is centered (neither right nor left) and the car is facing north. In Manhattan, all turns are exactly 90 degrees once initiated (U turns are not permitted). Your design is to be a **clocked synchronous circuit of the Moore form**. Assume the **clock signal CLK is derived from the left and right signals**.

(a) Provide a **state transition graph for a Moore implementation** of the compass. **Use the minimum number of states**.

(b) Provide a **state table** for the compass.

(c) Derive the **flip-flop input equations** and **compass output equations** for an implementation which uses **clocked D flip-flops**. Assume the INIT signal is used to reset the flip flops. Draw a **schematic diagram** for your circuit, including the D flip-flops and a minimum number of logic gates (no multiplexors!). **Show all Karnaugh maps used**.

2(a) (4pts) State Transition Graph:

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Department of Electrical Engineering
and Computer Sciences

CS 150 - Spring 1992
Prof. A. R. Newton

Quiz 2 Solutions

(1) (a) The binary string "**10110101**" is the **8-bit two's complement** representation of a fixed point number. **What is its decimal value**?

1(a) (5pts)

10110101 = ____-75__$_{10}$

(b) Design a circuit to compute the **two's complement** of a **3-bit binary number**. The inputs are b_0, b_1 and b_2, where b_2 is the most significant digit and the outputs are c_0, c_1 and c_2 where c_2 is the most significant digit.

(i) Show a **truth table** for the circuit.

(ii) Draw **Karnaugh maps for each output** and use them to simplify the functions.

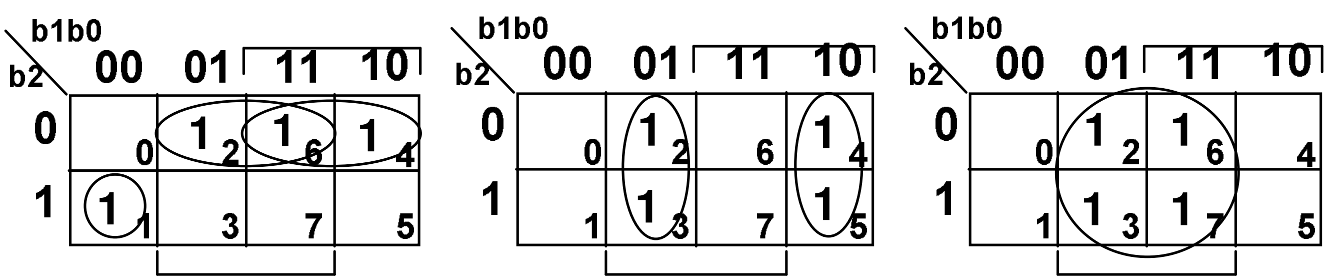
(iii) Draw a **schematic diagram** using the **minimum number of NAND gates and inverters only**.

1(b) (15pts)

(i) Truth table:

b_2	b_1	b_0	c_2	c_1	c_0
0	0	0	0	0	0
0	0	1	1	1	1
0	1	0	1	1	0
0	1	1	1	0	1
1	0	0	1	0	0
1	0	1	0	1	1
1	1	0	0	1	0
1	1	1	0	0	1

(ii) Karnaugh Maps:



c2 = b2'b0 + b2'b1 + b2'b1b0'

c1 = b1'b0 + b1b0'
= b1 xor b0

c0 = b0