Additional Space for Working Problems

Your Name: ____

Additional space for Problem 5

....

(b) (i) Find a hazard-free implementation of the following function using only 3-input NOR gates. Use the minimum number of gates+gate inputs and assume complements are available:

$f(A,B,C,D) = \Sigma m(0,2,6,7,8,10,13)$

(ii) Explain how a hazard in the next-state logic of a Mealy clocked synchronous machine can affect the performance of the machine adversely. Consider all cases and recommend ways of avoiding such adverse outcomes (other than simply eliminating the hazard by adding additional gates!)

(iii) What are the adverse effects which might result when one eliminates the hazard by adding additional gates?

5(b) (10pts)

(i) Hazard-free, three-input NORs only:

(ii)

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(iii)

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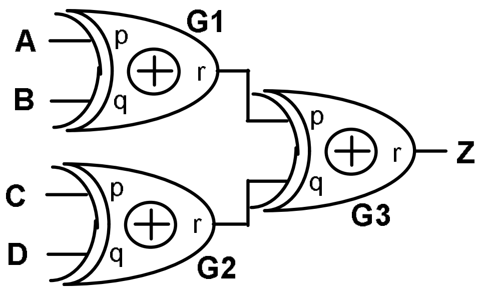
(5) (20pts)

(a) Consider the following four-input circuit:



(i) How many **conventional stuck-at-0 and stuck-at-1 faults** are there in this circuit?

(ii) How many **essential faults** are there in the circuit after fault implication and fault equivalences are considered? **List all of them by name.**

(iii) List the **minimum set of test patterns** needed to test for all essential single stuck-at-1 and stuck-at-0 faults in the network.

(iv) What patterns would you apply to determine specifically that the **particular stuck-at fault was actually the output G2.r stuck-at-1** (or the input G3.q stuck-at-1)? (i.e. fault diagnosis)

5(a) (10pts)

(i) Stuck-at-0: _________ **Stuck-at-1:** _________

(ii) Essential Faults: ____

____

(iii) Test Patterns:

A																
B																
C																
D																

(iv) Test Patterns:

A																
B																
C																
D																

Your Name: ____

(b) Consider the merged flow table shown opposite:
Perform a **race-free state-assignment** using as few internal state variables as possible. **Indicate all required adjacency constraints** and **list your final state codes.** Be *very* clear in explaining how you arrived at your result.

	Inputs AB			
	00	01	11	10
a	1	9	8	2
b	1	9	3	2
c	1	9	3	4
d	1	9	5	4
e	1	6	5	10
f	1	6	7	10
g	1	9	7	10
h	1	9	8	10

4(b) (10pts)

State assignment: ____

____

____

Adjacency constraints:

Additional Space for Problem 4

(4) (20pts)

(a) A two-button electrical lock will actuate according to the following sequence:

A:	0	1	1	1	1	0	1
B:	0	0	1	0	1	1	1
Z:	0	0	0	0	0	0	1

Z=1 opens the lock and is the circuit output while A and B correspond to the two buttons. A switch being depressed (pushed and held down) corresponds to a 1 and a switch being released (removing one's finger from the button) corresponds to a zero. Releasing both buttons clears the circuit and **only one button may be pressed or released at a time**, as is the case in the above sequence.

(i) Obtain a **primitive flow table** for the circuit.

(ii) Obtain a **reduced, merged flow table** by eliminating any redundant states and by merging equivalent states. **Show your merger diagram.**

4(a) (10 pts)

Primitive Flow Table:

Merger Diagram:

Reduced, Merged Flow Table:

Your Name: ____

3 (b) Consider the conventional D latch circuit below left and the alternative circuit shown on the right:

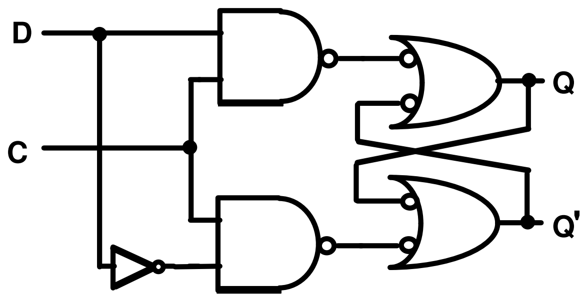


Fig. 1: Conventional D Latch

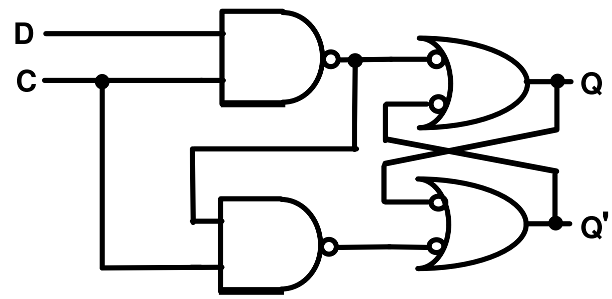


Fig. 2: Alternative Circuit

(i) **Prove that the circuit of Fig.2 is functionally equivalent to that of Fig. 1.**

(ii) **In what way(s) is the circuit of Fig. 2 actually better** from the standpoint of practical use? List all possible reasons that it is better.

3(b) (10 pts)

(i) Proof:

(ii) Reasons:

(3) (20pts)

Consider the following state table for a clocked, synchronous sequential machine, where "**-**" represents a "don't care" for the value of Z:

PS	NS, Z	
	x = 0	x = 1
A	A, **-**	B, 1
B	G, **-**	D, 0
C	B, 1	B, **-**
D	A, 1	B, **-**
E	C, **-**	A, **-**
F	F, **-**	C, **-**
G	G, **-**	G, **-**

(a) Obtain a **reduced state table** by eliminating redundant states and by combining equivalent states using the **implication chart method. Show your final implication chart** and include a final version of the **reduced state table with the minimum number of states.**

3(a) (10pts)

Implication Chart:

Reduced State Table:

2 (b) Derive a **combinational circuit** for realizing the **two's complement of a four-bit binary number.** Use the **minimum number of AND, OR, NAND, NOR, and XOR gates only**. Assume complements are available.

2(b) (10pts)

Additional Space for Problem2(b)

(2) (20pts)

(a) Design a circuit using **one-bit full-adders only** that may be used for **adding a column of six single-bit numbers** (i.e. each number can take only the value zero or one.) Show all working and **a schematic diagram** of you final circuit.

2(a) (10pts)

Additional Space for Problem2(a)

Your Name: ____

(b) Consider the following two functions expressed in Standard Sum-of-Products form:

$f_a(A,B,C,D) = \Sigma m(0,1,4,5,9,13,14,15)$

$f_b(A,B,C,D) = \Sigma m(0,4,5,7,9,13,14,15)$

(i) Does $f_a(A,B,C,D)$ contain a hazard when implemented in minimum sum-of-products form? If so, what product term should be added to remove it?

(ii) The functions are to be implemented together as a single two-output, four input logic circuit in sum-of-products form. Express each output in sum-of-products algebraic form, where the number of (AND gates+OR gates) needed is minimized. Do not consider the number of gate inputs in your calculation, just the total number of gates, and ignore any hazards (i.e. do not remove them, if present).

1(b) 7pts

(i) Is there a hazard in f_a? ________ **If so, what would you add?** ________________

(ii)

f_a(A,B,C,D) = ____

f_b(A,B,C,D) = ____

Additional Space for Problem 1

CD \ AB	00	01	11	10
00				
01				
11				
10				

CD \ AB	00	01	11	10
00				
01				
11				
10				

CD \ AB	00	01	11	10
00				
01				
11				
10				

Your Name: ____

(1)	/20
(2)	/20
(3)	/20
(4)	/20
(5)	/20
TOTAL	/100

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Department of Electrical Engineering
and Computer Sciences

CS 150 - Spring 1996
Prof. A. R. Newton

Final Examination

(Open Katz, Calculators OK, 3 hours)

Include all final answers in locations indicated on these pages. Use space provided for all working. If necessary, attach additional sheets by staple at the end. BE SURE TO WRITE YOUR NAME ON EVERY SHEET.

(1) (20pts)

(a) Consider the following logic function:

$f(A,B,C,D) = ABC + A\overline{B}\overline{C} + \overline{C}D$

(i) Express the function in **Standard Sum-of-Products** form.

(ii) Express the function as a **PLA table** using a **minimum number of product terms**.

(iii) What is the **minimum number of bits of storage** required to implement this function using a **ROM**? How many **address lines** would be required?

(iv) Implement the function using a **two control-line, four input multiplexer** and a **minimum number of additional logic gates (AND, OR, NAND, NOR, XOR)**. Assume complements are available and show all working.

1(a) 13pts

(i) f(A, B, C, D) = ____________________________________

(ii)

(iii) Number of bits: _________ **Number of address lines:** _________

(iv)