Your Name: ____

Additional space for Problem 6

(6) (17pts) Consider the following state table for a synchronous state machine:

Present State	input x=0	input x=1
a	a,0	e,0
b	c,0	b,1
c	a,0	f,0
d	c,0	b,1
e	f,0	e,0
f	a,0	f,0

(a) Reduce the table to the minimum number of states and show the reduced table.

6(a) (7pts)

(b) Find a good state assignment using the three guidelines mentioned in class for your reduced table. List all adjacency conditions and try to satisfy as many of them as possible.

6(b) (10pts)

Your Name: ______________________________________

(d) Provide a **schematic diagram** for the machine using a **minimum number of logic gates (AND, OR, NAND, NOR, XOR, XNOR, or inverters). Indicate your state variables as labels on buffer symbols**. Ensure that the **output logic cannot produce glitches and state why that is so. Assume input complements are available.**

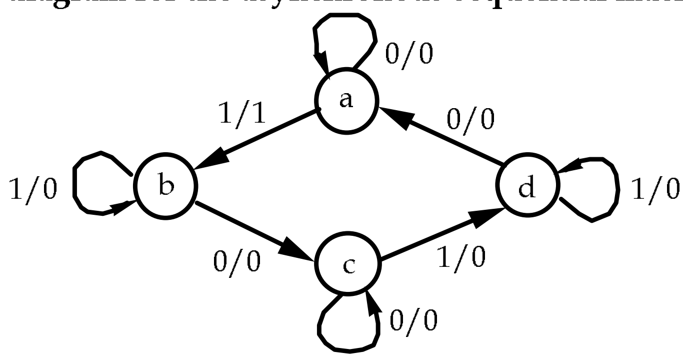
3(b) (6pts)

Additional space for Problem 5

(5) (18pts) (a) What problem can a **static hazard** cause in a **fundamental-mode asynchronous circuit**? How can the problem be avoided? List all possible solution techniques.

5(a) (4pts)

Consider the state diagram for the asynchronous sequential machine shown below.



(b) Draw a **primitive flow table** for the machine, indicating all stable states and outputs.

5(b) (4pts)

(c) **With the code for State a given as all 1's** derive a **race-free state assignment** for the machine using a **minimum number of internal state variables. Show all working.**

5(c) (4pts)

a = ______ b = ______ c = ______ d = ______

(c) Determine the **next-state and output equations** for your machine and **implement the circuit using positive edge-triggered D flip-flops** and a **minimum number of two-input NAND gates only.** Assume X comes from the output of another flip-flop and so the **complement of X is also available.**

3(b) (6pts)

Additional space for Problem 4

(4) (14pts) A clocked, synchronous sequential circuit is to be designed as follows:

"The circuit is to have a single input, X, that is used to control two outputs Z_1 and Z_2. At any time while X is 0, $(Z_1,Z_2) = (00)$. When X becomes 1, the outputs (Z_1,Z_2) begin the sequence (01, 11, 10), starting from the (00) state. If they reach the value 10 they hold that value until the input changes to 0 again."

(a) Construct a **state transition graph (STG)** for the machine in **Moore form.**

3(a) (4pts)

(b) **Convert your STG to Mealy form** and make a **state assignment that minimizes the amount of output logic** needed for a Mealy implementation of the machine.

3(b) (4pts)

Your Name: ______________________________________

(c) Use the reduced set of equations to **obtain a circuit diagram for an implementation of the machine.** Use the **minimum number of logic gates (AND, OR, NAND, NOR, XOR, XNOR, or inverters)** and **positive-edge-triggered J-K flip-flops only.**

3(c) (6pts)

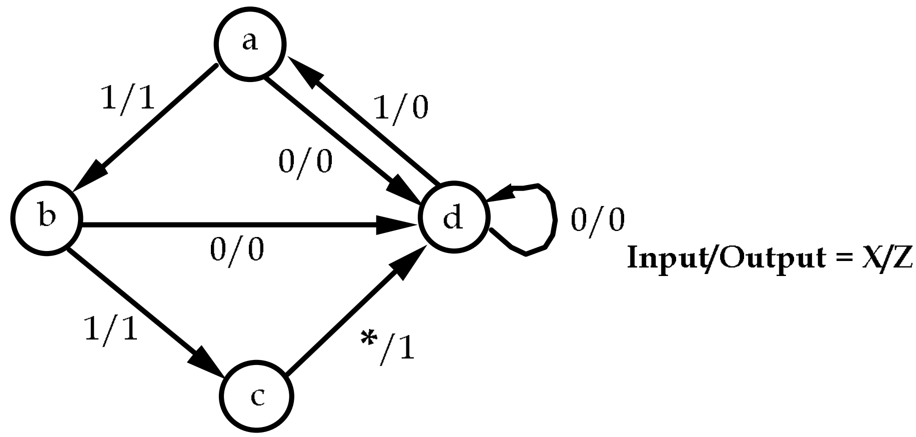
(c) **Using your next-state table from Part 3(a)** above, **construct an implication table** and check for state equivalence. **List the equivalent states. Enter the word NONE below if you cannot find any equivalent states from your table.**

3(d) (4pts)

Equivalent States: _____________

Additional space for Problem 3

(3) (19pts) Consider the following state-transition graph which is to be **implemented as a clocked, synchronous sequential circuit.** If State d is the reset state and the **states are encoded as State a = 01, State b = 11, State c = 10, and State d = 00**:



(a) Construct a **state transition table** for the machine in terms of **input** X and **present-state (y_1 y_2)** for **output** Z and **next-state (Y_1 Y_2.)**

3(a) (4pts)

(b) **Use Karnaugh map(s)** to obtain the **reduced next-state and output equations** for the machine. **Show your Karnaugh map(s.)**

3(b) (6pts)

(c) Implement the function using a **minimum number of simple logic gates (AND, OR, NAND, NOR, XOR, XNOR, and inverters only.)**

2(c) (4pts)

(d) Construct the **PLA-format table representation** for the function in **NOR-NOR form.** How many **product terms** would a NOR-NOR PLA implementation require?

2(d) (2pts)
Product terms: __________

(e) If the function were implemented using a ROM, **how many ROM storage locations** would be required? **How many address input lines** would the ROM have?

2(e) (2pts)		
	Storage Locations: _________	**Address inputs:** _________

Additional space for Problem 2

(2) (16pts) Consider the logic function shown below in Karnaugh Map form. In all parts to this question, **assume input complements are not available** (i.e. **an inverter counts as a gate**.)

f(A,B,C,D) =

CD \ AB	00	01	11	10
00	1	0	1	0
01	0	1	0	1
11	1	1	1	0
10	0	0	0	1

(a) Derive an implementation of this function using **a single 8-input, 3-control-line multiplexer and a minimum number of logic gates.**

2(a) (4pts)

(b) Derive an implementation of the function using **a single 4-input, 2-control-line multiplexer and a minimum number of two-input XOR gates and inverters only**.

2(b) (4pts)

(c) **Considering the first function $f_1(A,B,C,D) = \Sigma m(2,3,7,11,14,15) + \Sigma d(1,5,9,10)$ only**, draw a **schematic diagram for f_1 that uses the minimum number of logic gates.** Use **only NAND gates** and **assume input complements are available .**

1(c) 4pts

Additional space for Problem 1

Your Name: ______________________________________

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Department of Electrical Engineering
and Computer Sciences

CS 150 - Spring 1995
Prof. A. R. Newton

Special Final Examination

(Open Katz & assynch. notes only, Calculators OK, 3 hours)

Include all final answers in locations indicated on these pages. Use space provided for all working. If necessary, attach additional sheets by staple at the end. BE SURE TO WRITE YOUR NAME ON EVERY SHEET.

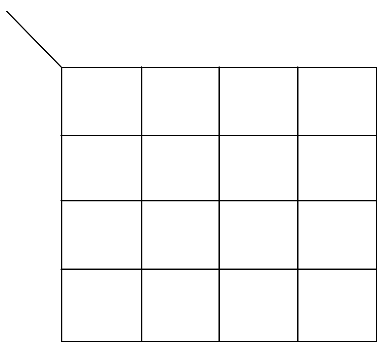
(1) (16pts) Consider the following logic functions expressed in standard sum-of-products form:

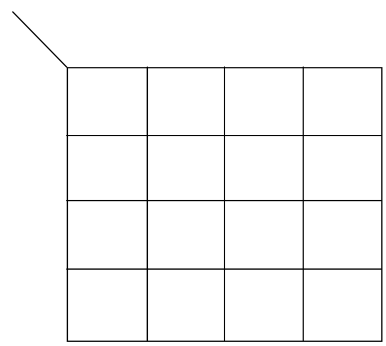
$f_1(A,B,C,D) = \sum m(2,3,7,11,14,15) + \sum d(1,5,9,10)$

$f_2(A,B,C,D) = \sum m(2,3,7,9,11,15)$

(a) Construct a **Karnaugh Map for each function** and write the **Boolean expression for each function as a minimum sum-of-products realization** (minimum number of (gates + gate inputs.)) **Show the product terms** you have chosen to implement each function **on the maps.**

1(a) 6pts

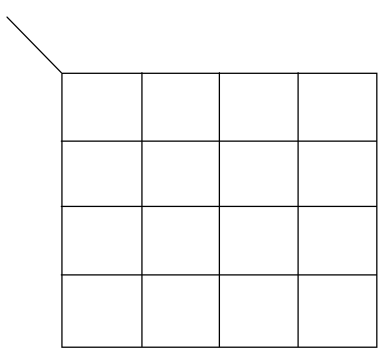


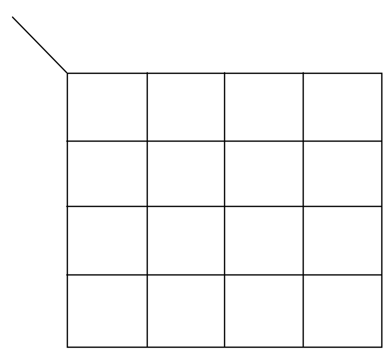


f_1(A,B,C,D) = ______________________ **f_2(A,B,C,D) =** ______________________

(b) If **the two functions are to be implemented together** (i.e. as a single, two-output, four-input function), construct a **Karnaugh Map for each output** and show the **product terms that represent the minimum number of (gates + gate inputs) for the combined, two-output function** on the maps. Write the **Boolean expression for each output.**

1(b) 6pts





f_1(A,B,C,D) = ______________________ **f_2(A,B,C,D) =** ______________________