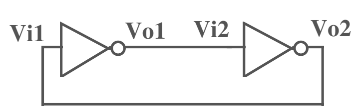
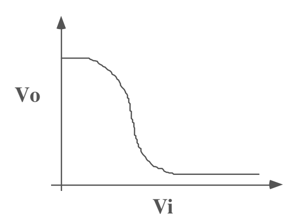
Outline

❍ Last time:
- ➜ Floating Point
- ➜ IEEE Formats
- ➜ Multiplication
- ➜ Division
- ➜ The Arithmetic Logic Unit (ALU)
- ➜ Bandwidth & Latency
- ➜ Scheduling & Allocation, Pipelining

❍ This lecture:
- ➜ Feedback in digital circuits
- ➜ Bistable and metastable circuits
- ➜ Review SR latch, D latch, flip-flops
- ➜ Master-slave flip flops
- ➜ JK Flip Flops
- ➜ Latch transformations

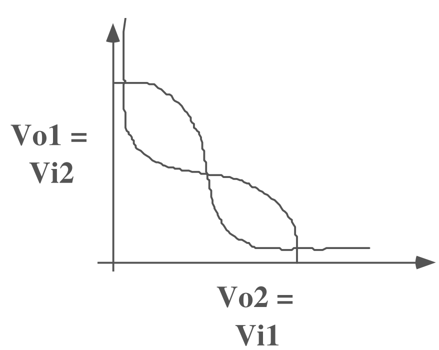
Feedback in Digital Circuits

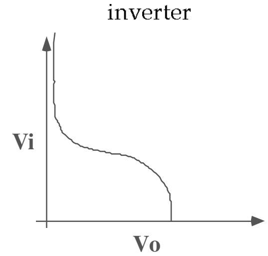




Vi2 = Vo1 = 0 1
Vi1 = Vo2 = 1 0

inverter

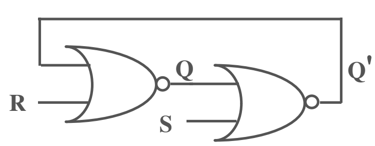


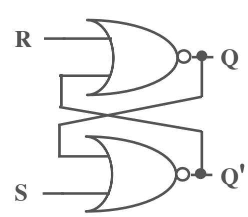


Latches and Flip-Flops

- Basic building-blocks of most sequential circuits
- Usual terminology:
  - ➜ *Flip-flop:* samples its inputs and changes its outputs at times determined by a "clocking signal."
  - ➜ *Latch:* Watches all of its inputs continuously and may change its outputs at any time.

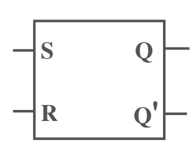
The Set-Reset (SR, RS) Latch



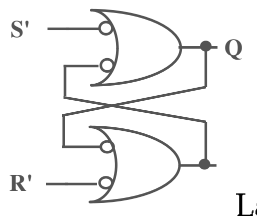


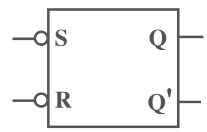
Latch Behavior

S	R	Q	Q'
0	0	last Q	last Q'
0	1	0	1
1	0	1	0
1	1	0	0



The S'-R' Latch

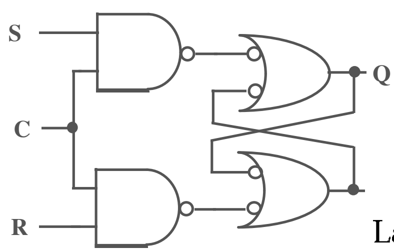


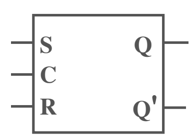


Latch Behavior

S'	R'	Q	Q'
0	0	0	0
0	1	1	0
1	0	0	1
1	1	last Q	last Q'

S-R Latch With Enable

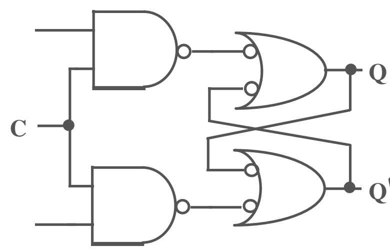




Latch Behavior

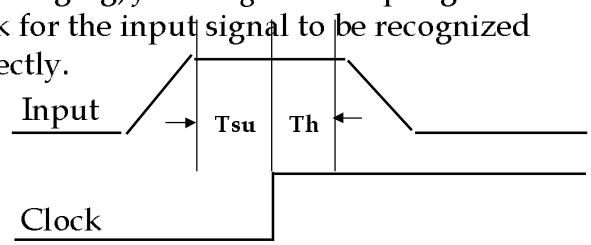
S	R	C	Q	Q'
0	0	1	last Q	last Q'
0	1	1	0	1
1	0	1	1	0
1	1	1	1	1
*	*	0	last Q	last Q'

Data (D) Latch

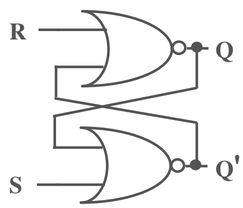


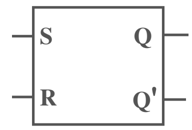
Review Setup and Hold Times

- **Setup Time (Tsu)** is the minimum time interval for which the input signal must be stable (unchanging) *prior to* the sampling event of the clock for the input signal to be recognized correctly.
- **Hold Time (Th)** is the minimum time interval for which the input signal must be stable (unchanging) *following* the sampling event of the clock for the input signal to be recognized correctly.



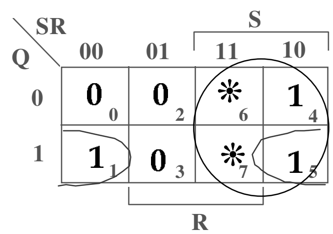
The Set-Reset (SR, RS) Latch





Latch Behavior

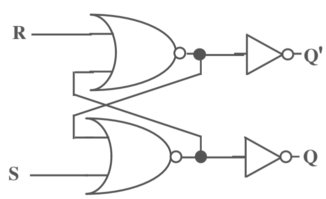
S	R	Q	Q'
0	0	last Q	last Q'
0	1	0	1
1	0	1	0
1	1	0	0



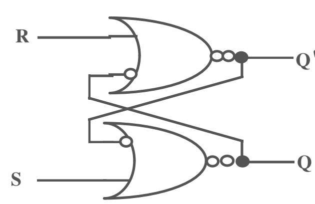
characteristic equation

$Q^{+} =$

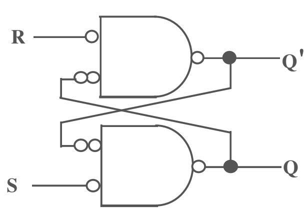
S-R Latch With NANDs



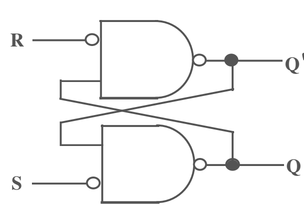
(a) Invert Outputs
(note: Q & Q' interchanged)



(b) Push inverters back

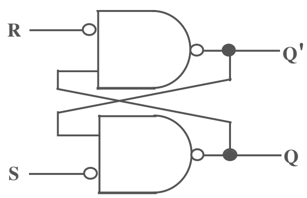


(c)De Morgan gates



(d) Remove unnecessary bubbles

S-R Latch With NANDs



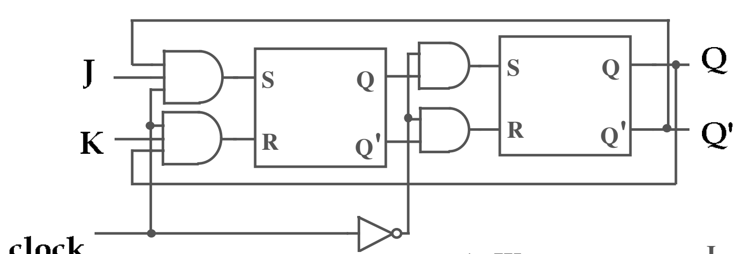
S	R	Qn+1	Qn+1'
0	0	Qn	Qn'
0	1	0	1
1	0	1	0
1	1	1	1

Q_n \ SR	00	01	11 (S)	10 (S)
0	0 (0)	0 (2)	1 (6)	1 (4)
1	1 (1)	0 (3)	1 (7)	1 (5)

R: columns 01, 11

Q_{n+1} =

The Master-Slave J/K Flip-Flop

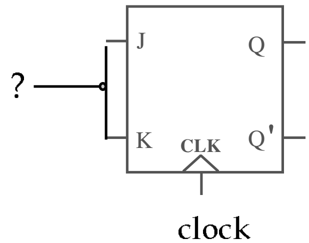


Q \ JK	00	01	11 (J)	10 (J)
0	(0)	(2)	(6)	(4)
1	(1)	(3)	(7)	(5)

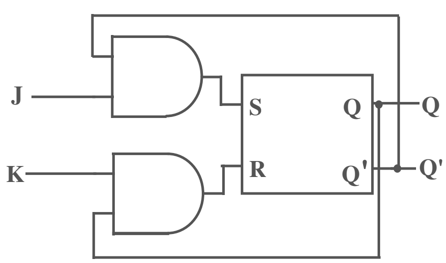
K: columns 01, 11

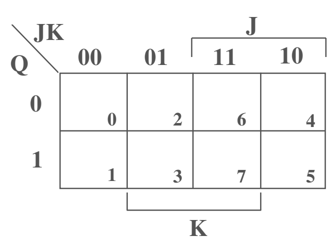
$Q^+ =$

J/K Flip-Flop
Conversions



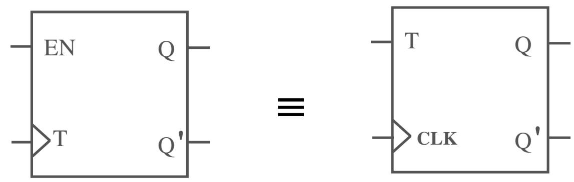
J-K Latch

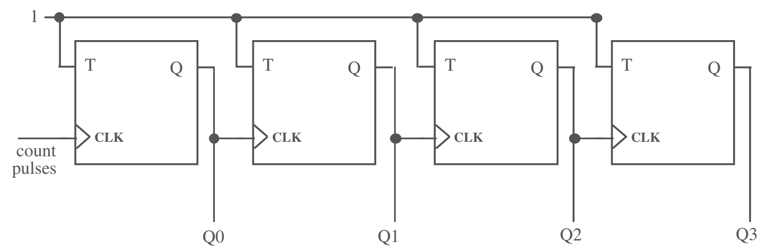




$Q^{+} =$

Flop





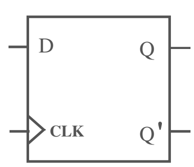
Latch & Flip-Flop Characteristic Equations

S-R Latch	Qn+1 = S + R'Qn
D latch	Qn+1 = D
Edge-triggered D Flip-Flop	Qn+1 = D
Master-slave S-R Flip-Flop	Qn+1 = S + R'Qn
Master-Slave J-K Flip-Flop	Qn+1 = JQn' + K'Qn
Edge-Triggered J-K Flip-Flop	Qn+1 = JQn' + K'Qn
T Flip-Flop	Qn+1 = Qn'
T Flip-Flop with Enable	Qn+1 = EQn' + E'Qn = E ⊕ Qn

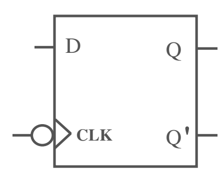
Input/Output Behavior of Latches and Flip-Flops

Type	When Inputs Sampled	When Outputs Valid	Tsu, Th Relative to:
Unclocked Latch	always	Tprop from input change	-
Level-Sensitive Latch	clock high	Tprop from input change	Falling clock edge
Positive edge triggered flip-flop	clock low → high transition	Tprop from rising clock edge	Rising clock edge
Negative edge triggered flip-flop	clock high → low transition	Tprop from falling clock edge	Falling clock edge
Master-slave flip-flop	clock high → low transition	Tprop from falling clock edge	Falling clock edge

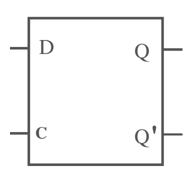
Standard Latch & Flip-Flop Conventions



Positive-Edge-Triggered D Flip-flop



Negative-Edge-Triggered D Flip-flop



D Latch with Enable