Outline

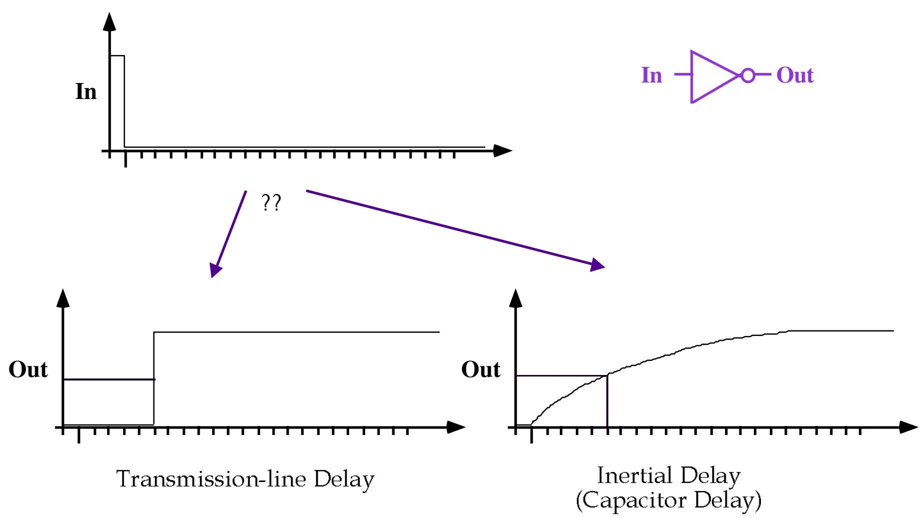
❍ Last time:
- ➜ Karnaugh Maps
- ➜ Relationship to Cube Notation
- ➜ Design Example: Simplify using Karnaugh Map
- ➜ Multiple-Output Karnaugh Maps
- ➜ "Dont Cares"
- ➜ Completely vs. incompletely specified logic
- ➜ Design Example: Use Karnaugh Map with "don't cares"

❍ This lecture:
- ➜ Implementation of logic functions: TTL, CMOS
- ➜ Delay models: Transition time, propagation delay
- ➜ Hazards and "Glitches"
- ➜ Hazard-free design
- ➜ Summary of combinational circuit design

Resistor-Transistor Inverter

CMOS Inverter

Inertial & Transmission-Line Delays



Transition Times

ideal

more realistic

tr **tf**

actual

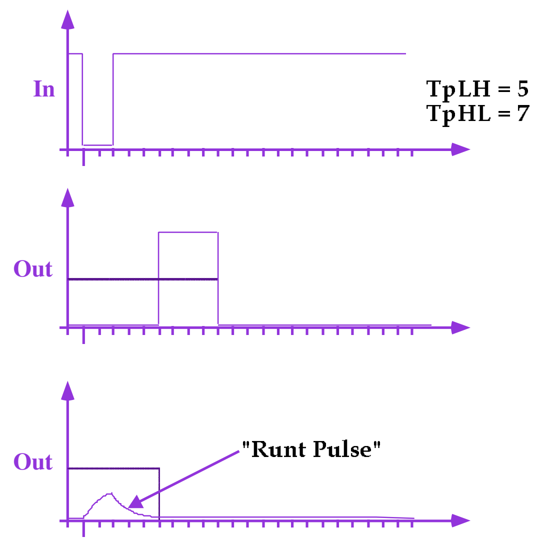
tr **tf**

Propagation Delay

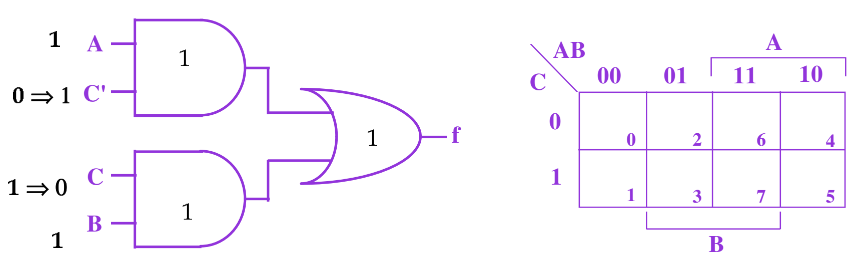
tpHL **tpLH**

tpHL **tpLH**

Pulse Propagation

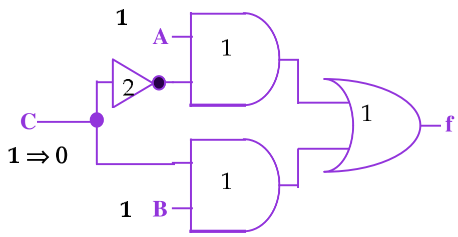


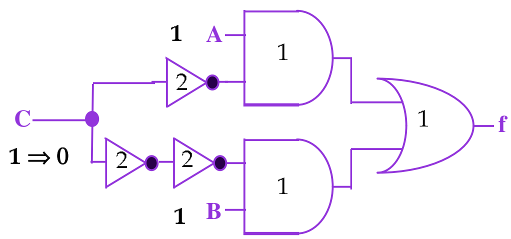
Hazards & Glitches



Remember: Eliminating a glitch in time saves nine!

Hazards & Glitches

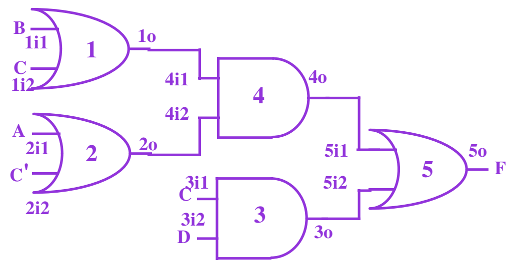




Hazards & Glitches

- A static-1 (static-0) hazard is the possibility of a circuit producing a glitch-to-0 (glitch-to-1). Hazards are a property of the implementation and have nothing to do with specific delay values.
- A dynamic-1 (dynamic-0) hazard is the possibility of a circuit producing a glitch-to-0 (glitch-to-1) when making the transition from 0 to 1 (1 to 0). That is, the sequence 0-1-0-1 (1-0-1-0) may occur.
- A glitch is the momentary transition of a signal from 0-1 or 1-0 in a circuit, usually caused by a hazard in the circuit. Glitches depend on the specific delays of logic gates.

Static and Dynamic Hazards



- static-1-hazard:

  a=0, b=1, d=1, c changing.

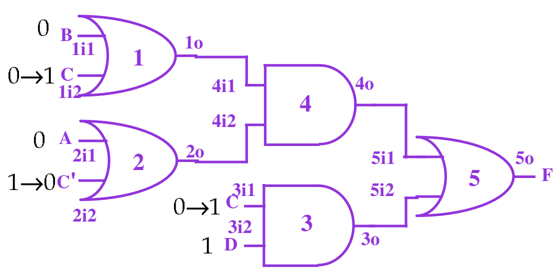
  Gate outputs: 2, 4, 5, 3, 5 (for c 0→1) or 3, 5, 2, 4, 5 (for c 1→0).

- static-0-hazard:

  a=0, b=0, d=0, c changing.

  Gate outputs - 1, 4, 5, 2, 4, 5 (c 0→1) or 3, 5, 2, 4, 5 (for c 1→0)

Dynamic Hazard



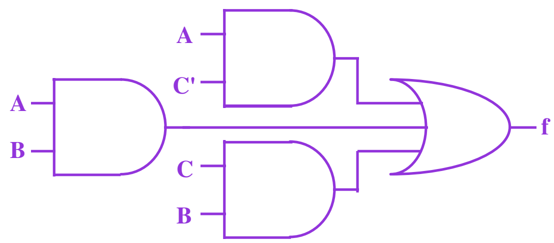
1o 0→1
2o 1→0
3o 0→1
4o 0
5o 0

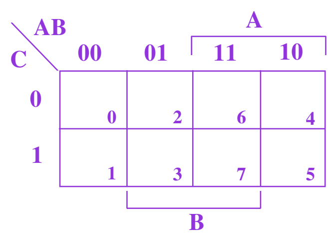
- A dynamic hazard is present under the condition:

  ABCD = 0001 → 0011.

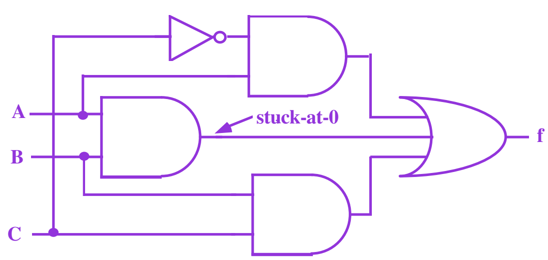
  If gate outputs switch in order - 1, 4, 5, 2, 4, 5, 3, 5 - it will produce a glitch at the output.

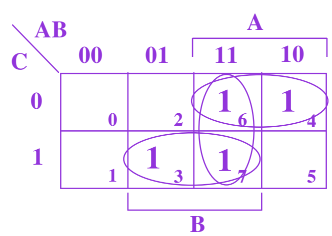
Hazards & Glitches





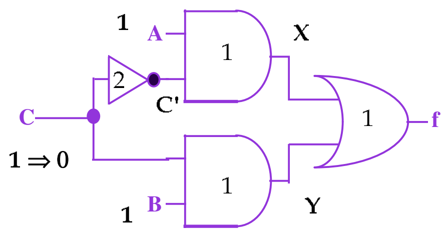
Aside: Redundancy & Testability

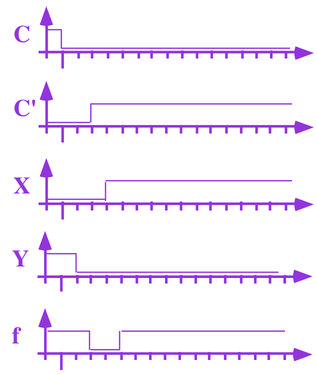




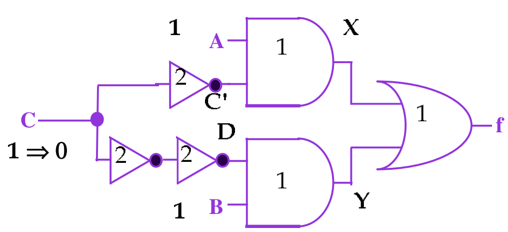
- Function fault types for testing:
  - ➜ Gate output or input "stuck" at logic 1 (stuck-at-1, SA1).
  - ➜ Gate output or input "stuck" at logic 0 (stuck-at-0, SA0).
  - ➜ Gate output or input open-circuit; wire not connected (open fault).
  - ➜ Short-circuit between wires (bridging fault)

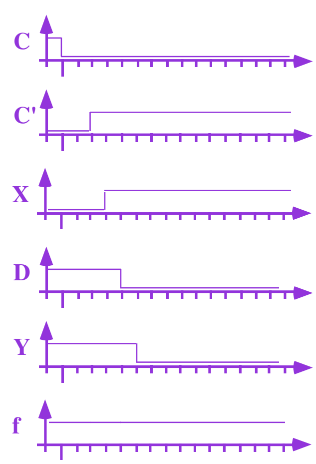
Timing Diagrams





Timing Diagrams





Timing Diagrams

Timing Diagrams

Causality arrows and propagation delays

Timing Diagrams

Uncertain or "don't know" delays

Timing Diagrams - Data

Certain and uncertain transitions

Timing Diagrams

Sequence of values on an 8-bit bus