Outline

- Last time:
  - VLSI Chips
- This lecture:
  - Where to from here?
  - The responsibilities of a technologist
  - CS150: once over lightly
  - Relationship to other courses in EECS

"I think there is a world market
for maybe five computers"
— Thomas Watson, Chairman of IBM, 1943

"There is no reason anyone would
want a computer in their home."
— Ken Olson, President & Founder, Digital

"Computers in the future may weigh
no more than than 1.5 tons."
— Popular Mechanics, 1949

"I have traveled the length and breadth of this country and have talked with the best people, and I can assure you that data processing is a fad that won't last out the year."

— The editor in charge of business books for Prentice-Hall, 1957

"But what... is it good for?"

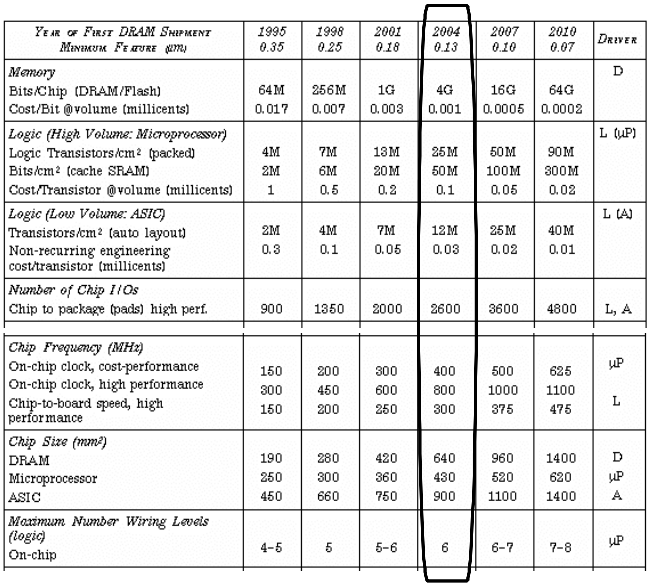
— Engineer at Advanced Computing Systems Division of IBM, 1968, commenting on the role of the microchip.

Semiconductor Industry Growth

		Steady State?
	1995	**2030**
Semiconductor as % of Electronics	**17%**	**35%**
Electronics as % of GWP	**4%**	**8%**
Semiconductors as % of GWP	**0.7%**	**3%**
CMOS Technology	**0.35µm**	**0.05µm**
World Semiconductor Sales	**$140B**	**$12,000B**
Annual Growth Rate	**16%**	**8%, same as GWP**

Source: Prof. Chenming Hu, UC Berkeley, 1996

SIA/SRC 1994 National Technology Roadmap



Year of First DRAM Shipment *Minimum Feature (µm)*	*1995* *0.35*	*1998* *0.25*	*2001* *0.18*	*2004* *0.13*	*2007* *0.10*	*2010* *0.07*	*Driver*
Memory							D
Bits/Chip (DRAM/Flash)	64M	256M	1G	4G	16G	64G	
Cost/Bit @volume (millicents)	0.017	0.007	0.003	0.001	0.0005	0.0002	
Logic (High Volume: Microprocessor)							L (µP)
Logic Transistors/cm² (packed)	4M	7M	13M	25M	50M	90M	
Bits/cm² (cache SRAM)	2M	6M	20M	50M	100M	300M	
Cost/Transistor @volume (millicents)	1	0.5	0.2	0.1	0.05	0.02	
Logic (Low Volume: ASIC)							L (A)
Transistors/cm² (auto layout)	2M	4M	7M	12M	25M	40M	
Non-recurring engineering cost/transistor (millicents)	0.3	0.1	0.05	0.03	0.02	0.01	
Number of Chip I/Os							
Chip to package (pads) high perf.	900	1350	2000	2600	3600	4800	L, A
Chip Frequency (MHz)							
On-chip clock, cost-performance	150	200	300	400	500	625	µP
On-chip clock, high performance	300	450	600	800	1000	1100	
Chip-to-board speed, high performance	150	200	250	300	375	475	L
Chip Size (mm²)							
DRAM	190	280	420	640	960	1400	D
Microprocessor	250	300	360	430	520	620	µP
ASIC	450	660	750	900	1100	1400	A
Maximum Number Wiring Levels (logic)							
On-chip	4-5	5	5-6	6	6-7	7-8	µP

Today's Design Methodologies
Will Not Scale Much Further

- **The Deep Sub-Micron (DSM) Effect ($\leq 0.25\mu$)**

$\propto$ DSM

"Microscopic Problems"

- **Wiring Load Management**
- **Noise, Crosstalk**
- **Reliability, Manufacturability**
- **Complexity: LRC, ERC**
- **Accurate Power Prediction**
- **Accurate Delay Prediction**
- **etc.**

Everything Looks a Little Different

?

$\propto$ 1/DSM

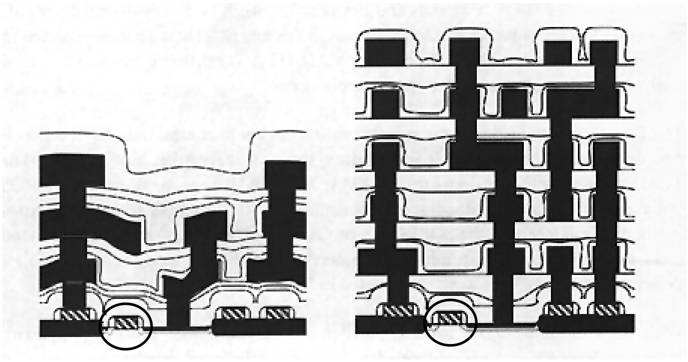
"Macroscopic Issues"

- **Time-to-Market**
- **Millions of Gates**
- **High-Level Abstractions**
- **Reuse & IP: Portability**
- **Predictability**
- **etc.**

...and There's a Lot of Them!

Adapted from Dr. Kurt Keutzer, Synopsys

Chip Interconnect Systems



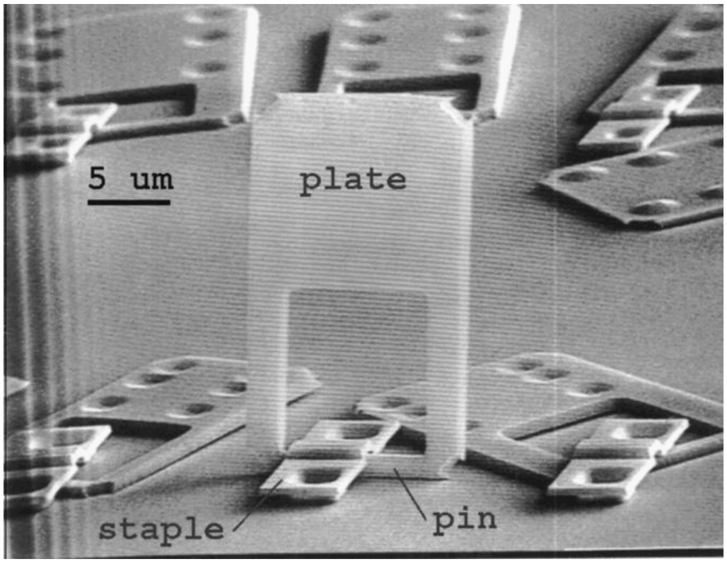
0.5 µm Rules **0.35 µm Rules**

IMEC Annual Report, 1996

◆ **New Design Methodologies: Wiring-Driven Everything!**

Routing-Driven Placement, Switch-Level Synthesis, Power, etc.

Chips That Fly?



Source: Dr. K. Pister, UCLA

Simplified Model of Design

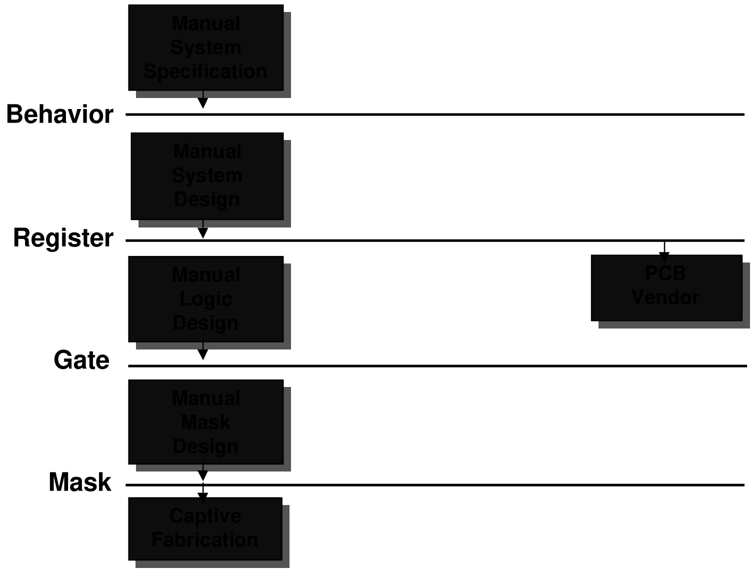
Behavior
Functions the system must implement
Time, area, power, etc. constraints
Implementation-independent description

Register
Components and their interconnections
Std. components & ROM, ASIC, PLD
Timing constraints for components

Gate
Low-level components & nets
In terms of ASIC library
EDIF well-suited to this description

Mask
Physical layout of IC or board
EDIF well-suited to this description

Evolution of Electronic Design Technology: 1970s



Manual System Specification

Behavior

Manual System Design

Register

Manual Logic Design

PCB Vendor

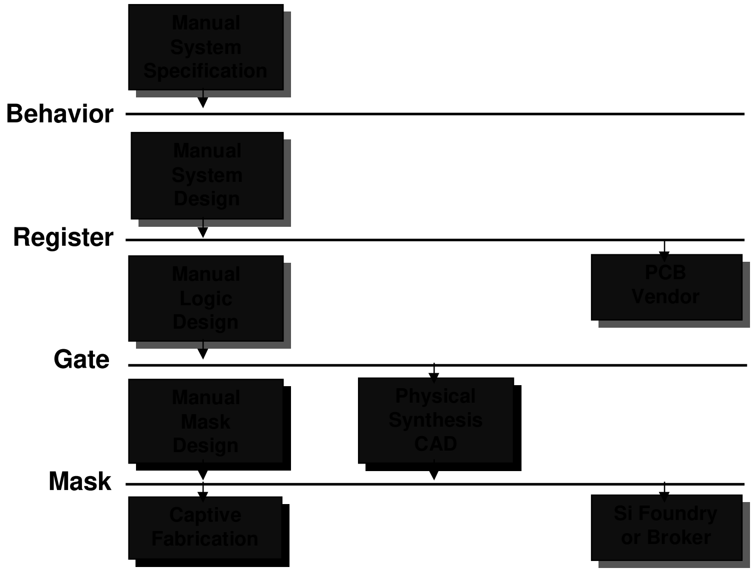
Gate

Manual Mask Design

Mask

Captive Fabrication

Evolution of Electronic Design Technology: Early 1980s



Manual System Specification

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Physical Synthesis CAD

Mask

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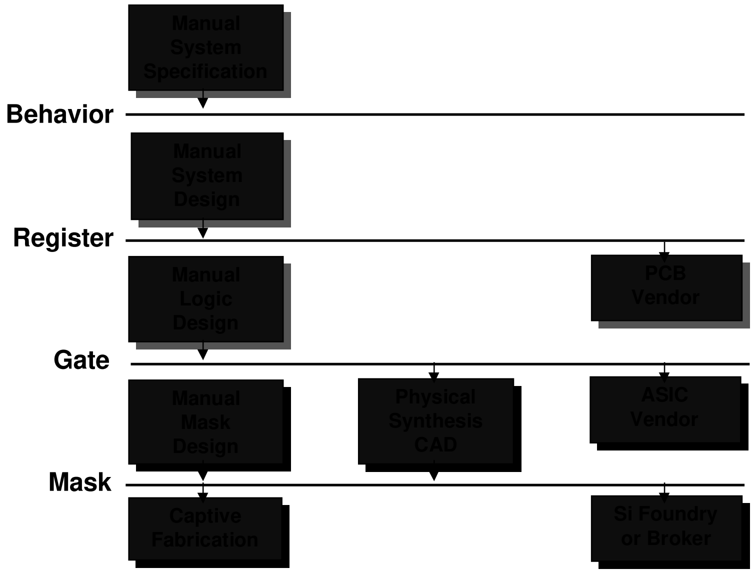
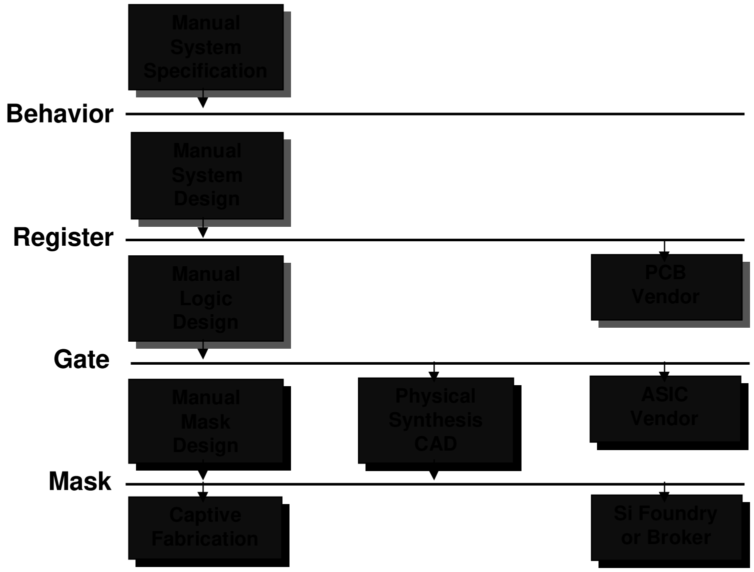
Si Foundry or Broker

Evolution of Electronic Design Technology: Mid 1980s



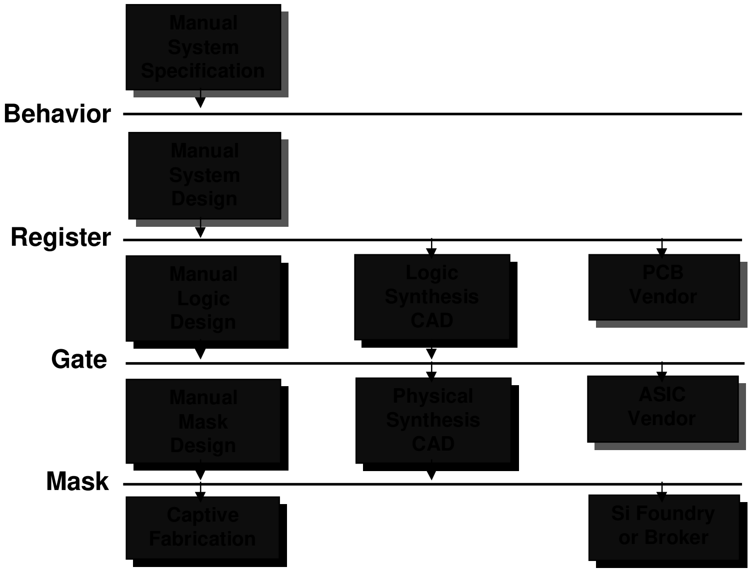
Evolution of Electronic Design Technology: Mid 1980s



Physical Design of VLSI Circuits

- ❍ **Mature Area for Low-Medium Performance ICs**
  - ➔ Specific developments remain for specific technologies (e.g. Sea-of-Gates)
  - ➔ Significant empirical development work remains
- ❍ **Procedural design still not successful, in general**
- ❍ **Timing-driven, multi-layer routing remains the major, outstanding problem.**
- ❍ **Next generation: General constraint-driven physical design.**
  - ➔ e.g. placement/path matching constraints for analog; path delay constraints for digital.

Evolution of Electronic Design Technology: Late 1980s



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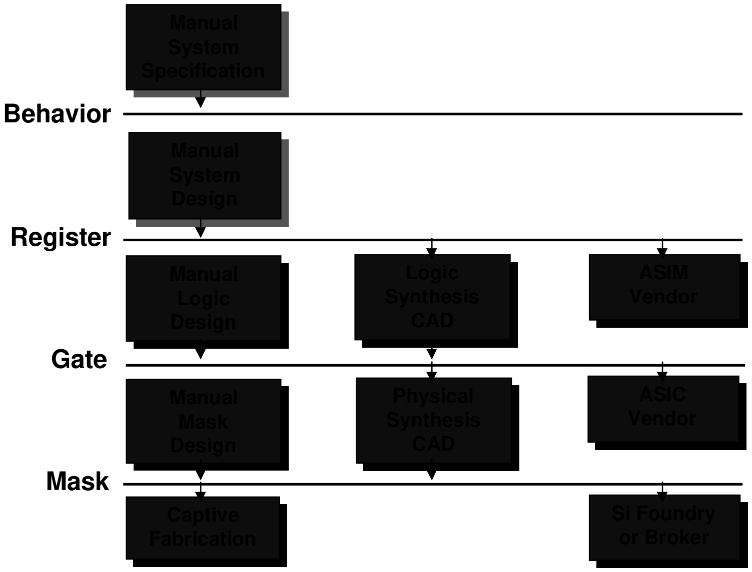
Profits Without Production

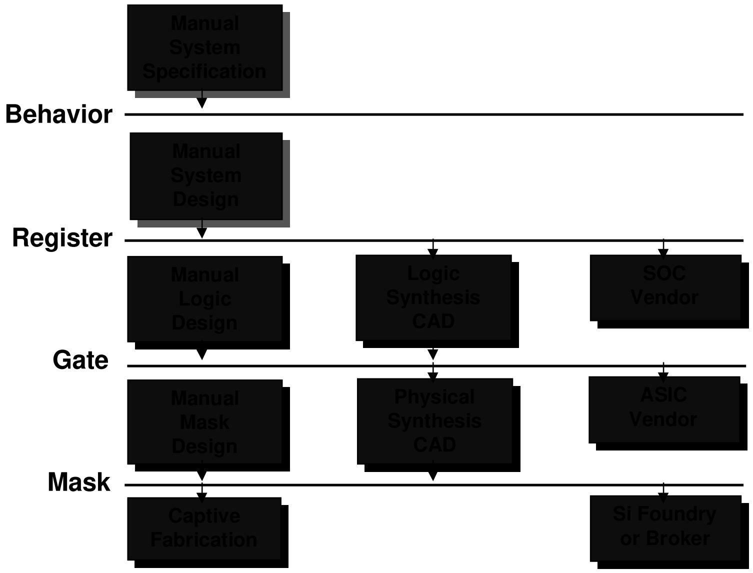
Company	Revenues 1990 ($M)	Net Income 1990 ($M)	Market Value	1990 Pretax ROI
Altera	78.3	13.4	324.9	34.0%
Ch.&Tech.	268.7	11.8	135.4	13.5%
Cirrus Log.	131.2	18.8	306.1	40.9%
Xilinx	83.7	13.9	506.9	26.7%
Weitek	57.8	7.0	108.8	30.1%
	619.7	64.9	1,382.1	26.4%

Source: Harvard Business Review
and TRG, July-Aug. 1991

Evolution of Electronic Design Technology: Early 1990s



Evolution of Electronic Design Technology: Late 1990s



Manual System Specification

Behavior

Manual System Design

Register

Manual Logic Design

Logic Synthesis CAD

SOC Vendor

Gate

Manual Mask Design

Physical Synthesis CAD

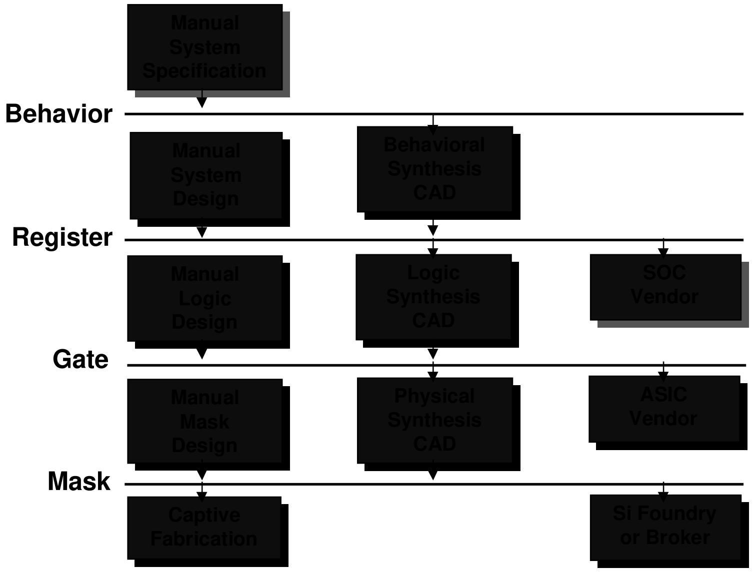
ASIC Vendor

Mask

Captive Fabrication

Si Foundry or Broker

Evolution of Electronic Design Technology: Early 2000's



Manual System Specification

Behavior

Manual System Design

Behavioral Synthesis CAD

Register

Manual Logic Design

Logic Synthesis CAD

SOC Vendor

Gate

Manual Mask Design

Physical Synthesis CAD

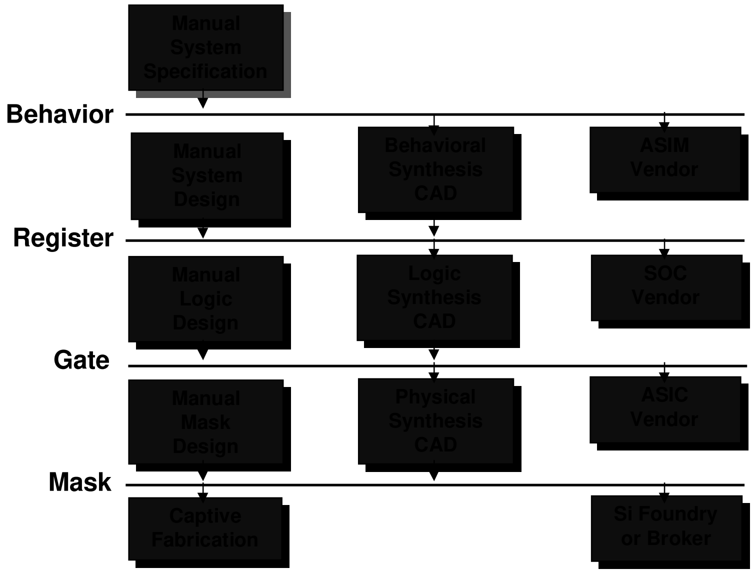
ASIC Vendor

Mask

Captive Fabrication

Si Foundry or Broker

Evolution of Electronic Design Technology: Early 2000’s



Manual System Specification

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Manual System Design

Behavioral Synthesis CAD

ASIM Vendor

Register

Manual Logic Design

Logic Synthesis CAD

SOC Vendor

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Physical Synthesis CAD

ASIC Vendor

Mask

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Si Foundry or Broker

Programmable Hardware

❍ Complex system-level products require extensive design verification

➔ Rapid prototyping and emulation

❍ Memory: Flash EEPROM

Logic: FPGAs

❍ Not just chips, but chip-interconnect as well...

❍ Design technology needs will be met by "synthesis" companies

FPGA Usage

- Design:
  - ➔ Total control over design cycle
  - ➔ Negligible NRE costs
  - ➔ Rapid prototyping
    - Debug/Prototype tool for complex designs
    - "Quick-Turn/Pie"-like emulation
  - ➔ Provides evolution path to gate-arrays

- Manufacturing:
  - ➔ Time-to-market
  - ➔ Multiple source, off-the-shelf components
  - ➔ Flexibility in adjusting functions for just-in-time production or field upgrades

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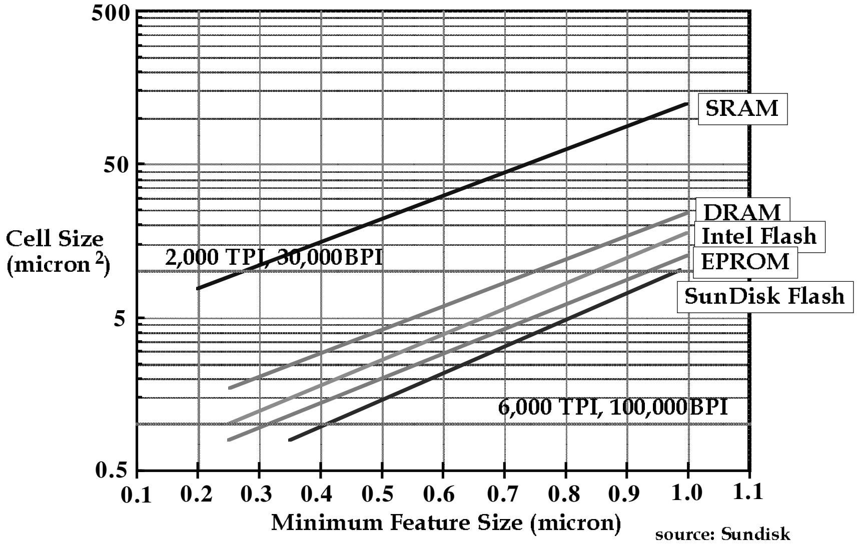
Cell Size vs. Minimum Feature Size for Flash E^{2}PROM



source: Sundisk

Next Development: FP Boards?

Chip

- **Full Custom**
- **ASIC**
  - **Gate Array**
  - **Standard Cell**
  - **Macrocell**
  - **Sea-of-Gates**
- **Standard Component**
- **FPGA/PLD**

Substrate

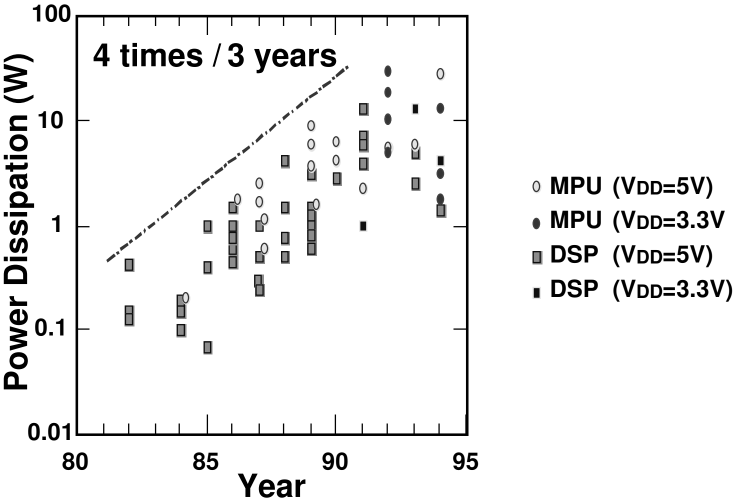
- **Full Custom**
- **Substrate Vendors**
  - **Wire-wrap/Multiwire**
  - **"Easy" Boards**
  - **"Advanced" Boards**
  - **MCM**
- **Standard Subsystem/Module**
- ***Field Programmable***

The Future of First-Level Packaging: Déja Vu?

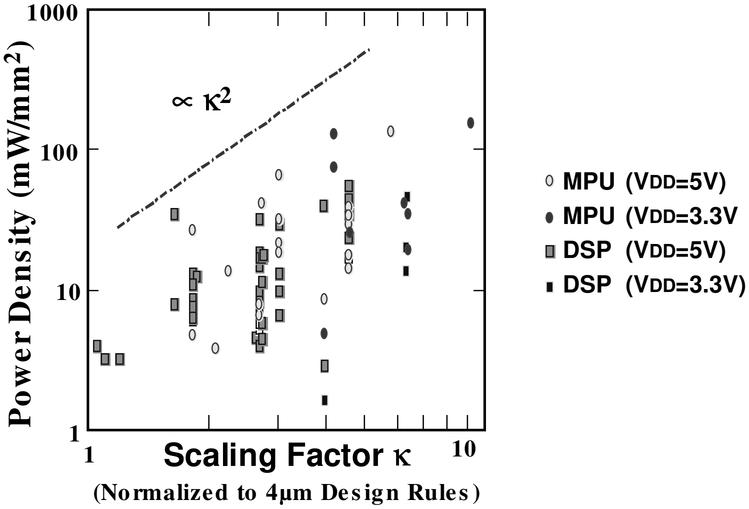
❍ **Boards are becoming increasingly sophisticated (e.g. < 4mil lines & spaces, MCMs, COB)**

- ➔ **Off-shore quotes up to 10x lower price**
- ➔ **20% reduction in number of independent US PCB suppliers from 1989-90.**

❍ **With very high cost of semiconductor fabrication, first-level package provides strategic product value-added to high-volume standard components**



Sakurai & Kuroda, Sashimi '96



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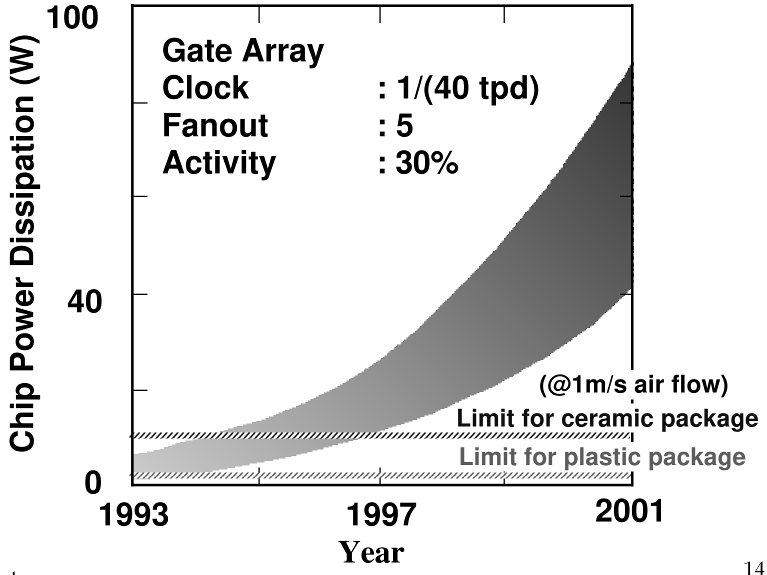

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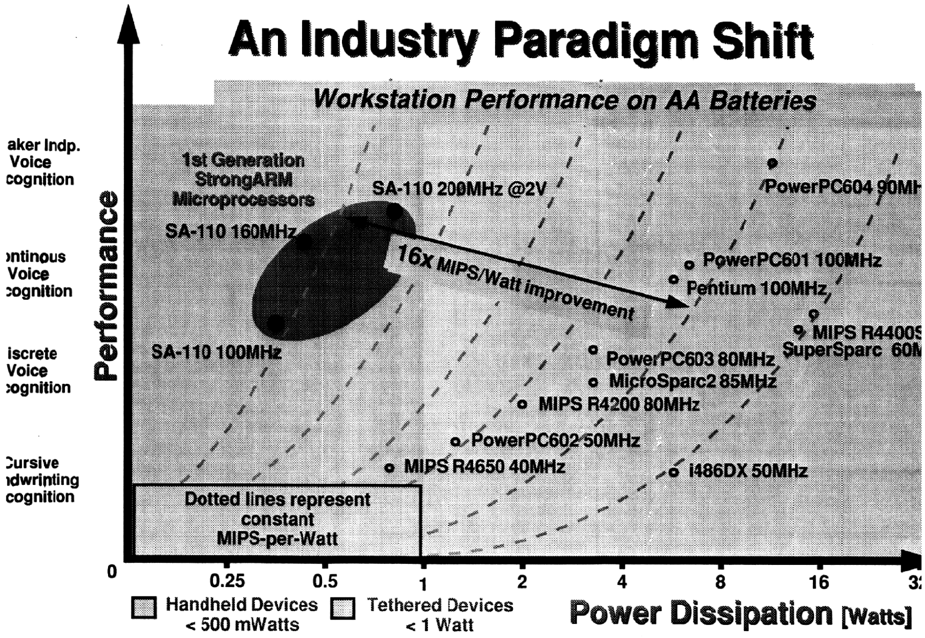
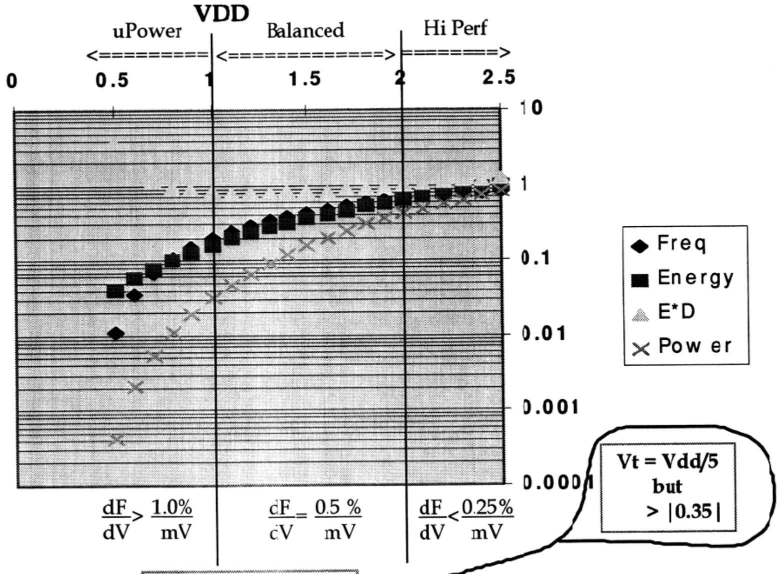

An Industry Paradigm Shift

Dan Dobberpuhl, Digital, Nov. 96

Choosing Vdd

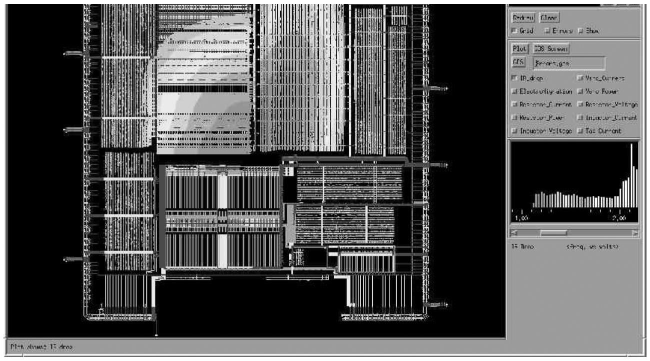


Vt = Vdd/5
but
> |0.35|

Vt is constrained

Dan Dobberpuhl, Digital, Nov. 96

Full-Chip Visualization of Complex Properties



- **6Mx6M dynamic linear matrix solution**
- **Need 100Mx100M over the next 5 years**