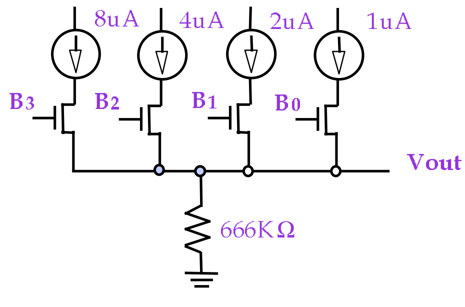
Outline

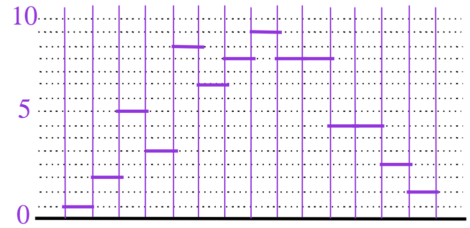
- Last time:
  - ➔ Combinational Testability and Test-pattern Generation
  - ➔ Faults in digital circuits
  - ➔ What is a test? : Controllability & Observability
  - ➔ Redundancy & testability
  - ➔ Test coverage & simple PODEM ATPG
  - ➔ Sequential Test: What are sequential faults?
  - ➔ SCAN Design
- This lecture:
  - ➔ Analog-Digital & Digital-Analog Conversion

Digital-to-Analog Conversion

Must create values proportional to the weight of each bit, then sum them in an analog way. One approach, use KCL (EECS 104): sum of currents entering a node is 0, then convert current to a voltage using a resistor. Ratioed currents obtained by scaling widths of transistors in a current mirror.

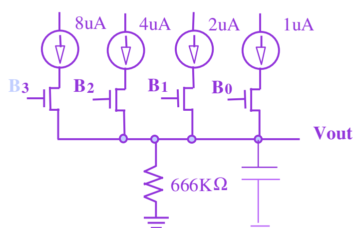


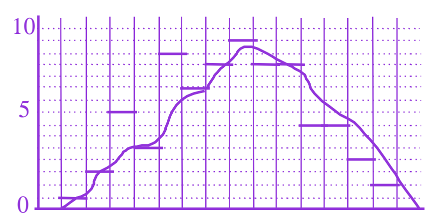
Digital-to-Analog Conversion



B0	0	1	1	0	1	1	0	0	0	0	0	1	1	0	0	0
B1	0	0	1	0	0	0	1	0	1	0	0	1	1	0	1	0
B2	0	0	0	0	1	1	0	1	1	1	1	1	1	1	0	0
B3	0	0	0	1	0	1	1	1	1	1	1	0	0	0	0	0

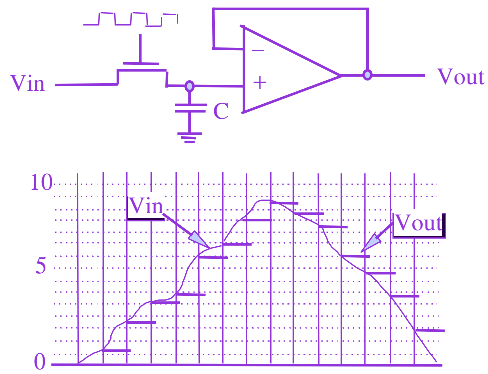
Digital-to-Analog Conversion



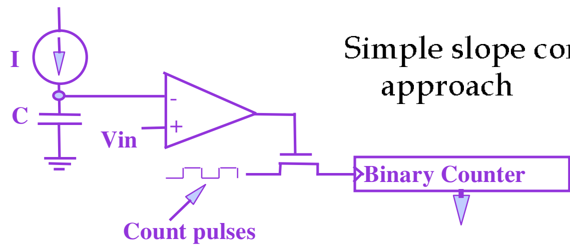


Use capacitor, or other form of low-pass filter, to smoothe response. Note: compromise!

Analog-to-Digital Conversion: Sample-and-Hold



Analog-to-Digital Conversion: Conversion to Binary



Simple slope conversion approach