

**University of California at Berkeley**  
**College of Engineering**  
**Department of Electrical Engineering and Computer Sciences**

EECS150  
Spring 2000

J. Wawrzynek  
E. Caspi

Quiz #7 – Solution

Using two memory ports, the following design simultaneously accesses both components of each linked-list element. The pointer component (address NEXT) is accessed via port b, while the value component (address NEXT+1) is accessed via port a.

Available components:

- 8 and 16-bit registers with synchronous clear (CL)
- 16-bit adder
- 8-bit zero-comparator

