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Quiz #6 – Solution

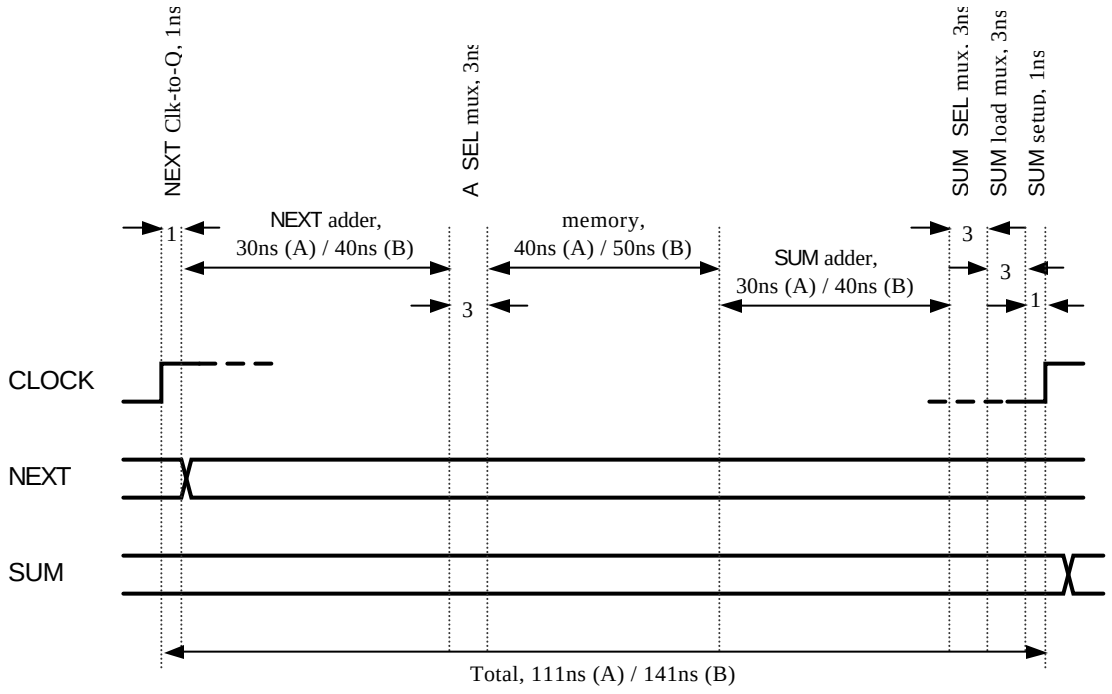
The critical path remains in the COMPUTE_SUM state. It is the path from NEXT through memory to SUM. Some of the given components have a width mismatch with respect to the original design spec from lecture, but we must use them anyway. We use a wastefully wide 16-bit adder to increment NEXT and a parallel pair of 8-wide multiplexors on the input to SUM. Note that the parallel composition of 2 multiplexors has exactly the same delay as one multiplexor. The total delay of COMPUTE_SUM, hence the minimum clock cycle, is either **111ns** or **141ns**, depending on your version of the quiz. Two versions were distributed, each with different timing for components.

Timing for quiz (A)

Component	Delay
8-bit Register	Clk-to-Q=1ns Setup=1ns
8-bit wide 2-1 Mux	3ns
16-bit Adder	30ns
Memory	40ns
Zero Comp are	5ns

Timing for quiz (B)

Component	Delay
8-bit Register	Clk-to-Q=1ns Setup=1ns
8-bit wide 2-1 Mux	3ns
16-bit Adder	40ns
Memory	50ns
Zero Compare	5ns



Timing diagram for COMPUTE_SUM state