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EECS150 Spring 2000 J. Wawrzynek E. Caspi

## Quiz #5 – Solution

In our simplified transistor model for digital applications, a transistor acts as a switch controlled by the gate voltage. When on, a transistor provides a resistive path between source and drain. When off, the source to drain path has high impedance ("high Z") and is effectively an open circuit. N-type transistors (nfets) can reliably transmit a 0 signal, whereas P-type transistors (pfets) can reliably transmit a 1 signal. To transmit either logic level, we need an nfet-pfet pair in parallel, commonly called a *transmission gate*.



With this model, the analysis of a digital transistor circuit comes down to determining which transistors are on and off. Analysis of the quiz circuit is shown below. Note that the structure in the middle (between x and y) is a transmission gate which is on when b=0 and off when b=1.



а	b	$t_1$	$t_2$	t <sub>3</sub>	t4	t <sub>5</sub>	t <sub>6</sub>	х	У	t7	t <sub>8</sub>	F
0	0			$\checkmark$	$\checkmark$			1	1		$\checkmark$	0
1	0			$\checkmark$	$\checkmark$	$\checkmark$		0	0	$\checkmark$		1
0	1		$\checkmark$				$\checkmark$	1	0			Hi Z
1	1		$\checkmark$			$\checkmark$	$\checkmark$	1	0			Hi Z

Truth table for quiz circuit

The truth table shows that the circuit operates in two modes, depending on b. When b=0, the output is F=a. When b=1, the output is in high impedance mode. This is precisely the function of a *tri-state buffer* with input a and control b.



## Extra credit:

This tri-state implementation might be preferred to the one presented in class (2/15/00 lecture notes, page 10.3) because it can be *smaller*. Understanding this requires understanding the typical use of tri-state buffers and knowing a bit more about transistors.

Tri-state buffers are typically used to write to long busses with high capacitance. That high capacitance comes from a bus's length and the sometimes large number of components connected to it. The speed at which a tri-state can write to a bus, *i.e.* switch its voltage level, depends on the RC time constant. In this case, C is the bus capacitance, and R is the output of the tri-state, namely the resistance of whichever transistor is driving the bus ( $t_7$  or  $t_8$ ). To switch the bus fast, those transistors need as low a resistance as possible, which means they must be large. The source-to-drain resistance of an on transistor is inversely proportional to its width, so those transistors must be wide (see MOSFET layout in 2/15/00 lecture notes, page 10.1). So wide, in fact, that those drivers determine the overall size of the tri-state.

Now compare with the tri-state implementation presented in class (2/15/00 lecture notes, page 10.3). In that circuit, the path from  $V_{DD}$  or GND to the output passes through two transistors in series. Because series resistances add, achieving a given resistance through those 2 transistors requires each transistor to be twice as wide. Thus, when designing a tri-state with a given output resistance, the class implementation requires twice as many driving transistors, each twice as large, as the quiz implementation – it is four times as large.

Keep in mind that the driving transistors are typically the largest ones in a tri-state implementation, hence they determine its overall size. Although the quiz implementation has more transistors than the class implementation, it can be significantly smaller because of the difference in driver sizes.