

**University of California at Berkeley**  
**College of Engineering**  
**Department of Electrical Engineering and Computer Sciences**

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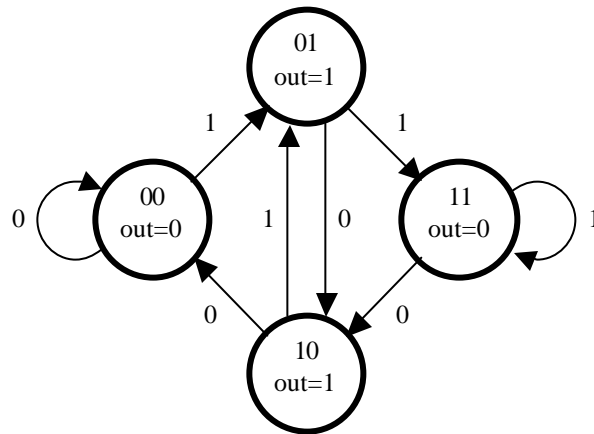
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Quiz #2 – Solution

The state machine has 4 states representing the two most recent input values: 00, 01, 10, 11. States 01 and 10 indicate an input change, whereas states 00 and 11 indicate no change. The FSM output is simply an OR of two state registers:

- “01 OR 10” if your quiz requested outputting 1 on a change
- “00 OR 11” if your quiz requested outputting 1 on no change.

Here is the state diagram:  
(assuming we output 1 on a change)



The one-hot-encoded logic circuit is readily derived from the state transition diagram. Each state gives rise to one flip flop, whose input is the OR of several AND gates representing the transition arcs coming into that state. Each such AND gate computes the AND of the previous state and input value (In or In') for its corresponding transition arc. The circuit diagram follows:

