

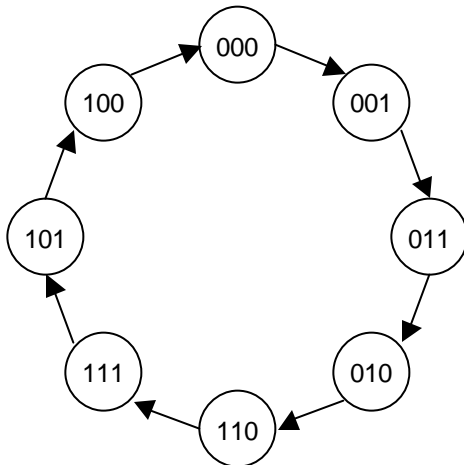
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Quiz #12 – Solution

The counter FSM will represent the gray-code directly in 3 state bits. The next-state function will be the “next gray-code” function, and the counter output will be the state registers.



State Transition Diagram

State			Next State		
S ₂	S ₁	S ₀	NS ₂	NS ₁	NS ₀
0	0	0	0	0	1
0	0	1	0	1	1
0	1	0	1	1	0
0	1	1	0	1	0
1	0	0	0	0	0
1	0	1	1	0	0
1	1	0	1	1	1
1	1	1	1	0	1

State Transition Table

S ₁ S ₀		00	01	11	10
S ₂	0	1	1	0	0
	1	0	0	1	1

$$NS_0 = S'_2S'_1 + S_2S_1 = (S_2 \oplus S_1)'$$

S ₁ S ₀		00	01	11	10
S ₂	0	0	1	1	1
	1	0	0	0	1

$$NS_1 = S'_2S_0 + S_1S'_0$$

S ₁ S ₀		00	01	11	10
S ₂	0	0	0	0	1
	1	0	1	1	1

$$NS_2 = S_2S_0 + S_1S'_0$$

Karnaugh Maps for Next State

Reduced Logic Eqns