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EECS150
Spring 2000
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## Quiz \#10 - Solution

The carry-select scheme splits the 16-bit adder into four 4-bit quarters. Each quarter except the least-significant one is duplicated, computed once with a carry-in of 0 and once with a carry-in of 1 . The critical path is 10 cycles: 4 cycles to the carry-out of the least-significant quarter, plus 2 cycles for each of 3 cascaded multiplexor pairs on the way to $S[15: 12]$ and $C_{o u t}$.

Carry-Lookahead Adder
S: 3 gate delays $\mathrm{C}_{4}$ : 4 gate delays

Multiplexer
2 gate delays

Build this:
S: $\quad-\quad \mathbf{1 0}$ gate delays
$\mathrm{C}_{\text {out: }} \quad \underline{\mathbf{1 0} \text { gate delays }}$


