University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Sciences

EECS150 J. Wawrzynek
Spring 2000

Homework #9

This homework is due on **Friday April 14th by 11am**. Homework will be accepted in the EECS150 box on the door to room 218 Cory Hall. Late homework will be penalized by 50%. No late homework will be accepted after the solution is handed out.

All the following problems are from the **Katz book**:

Multi-Bit Adders	5.13(a,b)
Carry Select Adder	5.14
Combinational Multiplier	5.25, 5.27

Bit-serial Multiplier

Using the principle similar to those used in the bit-serial adder and the shift-and-add multiplier presented in class, design the data-path for a *bit-serial 4-bit unsigned multiplier*. Your circuit should use one flip-flop, several shift registers, and only one full-adder cell. Draw the circuit diagram and write down the control algorithm. How many cycles does your circuit take to perform 4-bit multiplication?