University of California at Berkeley College of Engineering Department of Electrical Engineering and Computer Sciences

EECS150 Spring 2000 J. Wawrzynek

Homework #6

This homework is due on **Friday March 10th by 11am**. Homework will be accepted in the EECS150 box on the door to room 218 Cory Hall. Late homework will be penalized by 50%. No late homework will be accepted after the solution is handed out.

This homework is based on the design example presented in class during the week of Feb. 21. Your first assignment is to review the class notes and make sure you understand them.



The design example can be simplified if we specify that the linked list must be stored in memory with the pointer field of each element in the list is aligned to a 16-bit (2-byte) boundary. An example of such a list is shown to the left.

1. Consider how you can simplify the data-path of architecture #1 from the class notes to take advantage of the new memory layout constraint. Redraw the data-path to reflect this simplification.

2. Redraw the detailed timing diagrams for the appropriate affected states. Recalculate the new maximum clock frequency.