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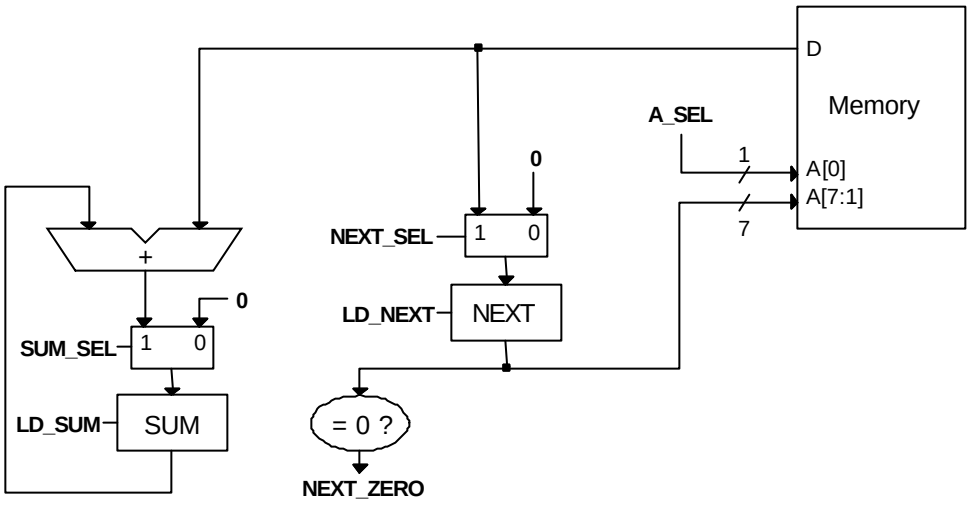
Homework #6 – Solution

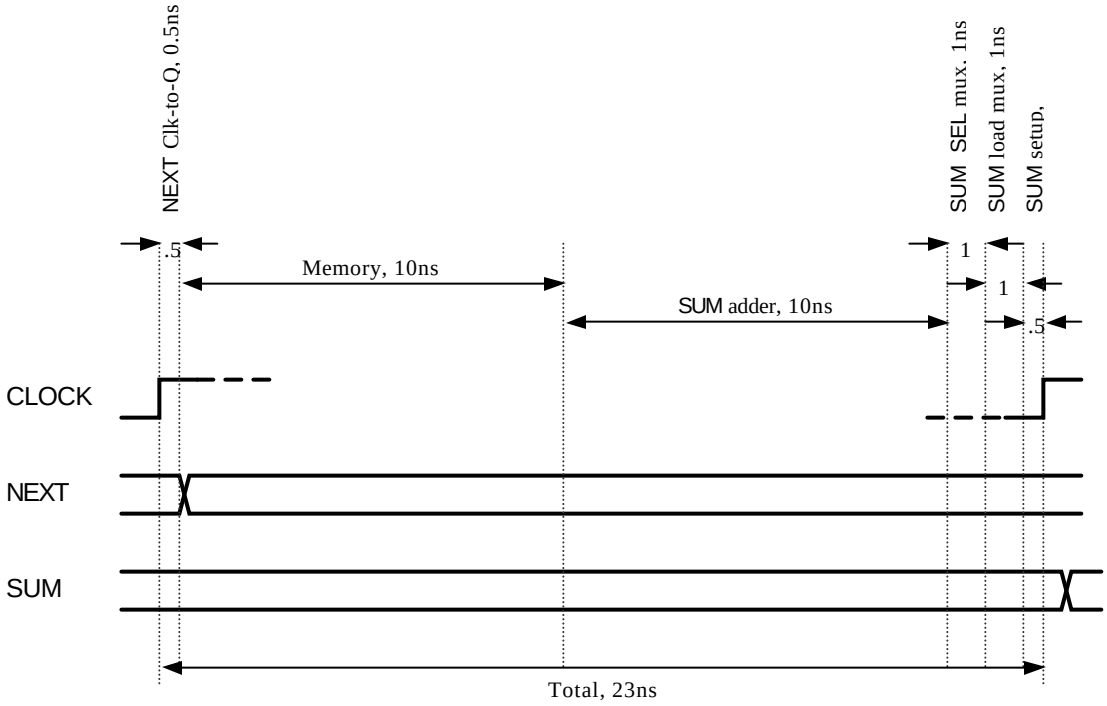
Aligning linked-list entries at 16-bit boundaries means that the addresses used to read an entry are *XXXXXXX0* and *XXXXXXX1*. This memory layout obviates the need for the 8-bit adder which increments the NEXT address as well as the mux which chooses NEXT or NEXT+1. Instead, NEXT will provide the upper 7 bits of the address (*XXXXXXX*), and A_SEL itself will provide the address LSB.



The GET_NEXT state is affected minimally, since the only effect of this optimization is to remove the 8-bit multiplexer from the path of NEXT to memory. Thus GET_NEXT is shortened by 1 cycle.

The COMPUTE_SUM state is significantly shortened, since this optimization removes an 8-bit adder and an 8-bit multiplexer from the path of NEXT to memory. This is a savings of 8+1=9ns from the critical path. COMPUTE_SUM remains the longest state at 23ns, setting the minimum clock period at **23ns** and the maximum frequency at **43.5MHz**. The timing diagram follows on the next page.

Note that this circuit has a bug! The input to the zero comparator should not be coming from the output of NEXT; it should be coming from the input to NEXT (*i.e.* from the NEXT_SEL multiplexor output). According to the state transition diagram from lecture, the comparator is used while state GET_NEXT is active, *before* the new NEXT value is latched into the register. If the comparator reads the output of the NEXT register, it is reading an old, irrelevant value. Instead, it must read the input to NEXT.



Timing diagram for COMPUTE_SUM state