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EECS150
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Homework \#2 - Solution

1. Here is the 4-bit parallel-to-serial converter shown in class:


Using positive edge-triggered flip-flops, FFs will record a new value on each rising clock edge. Let us consider what happens on each rising clock edge. If "LD" (load enable) is high, each FFs loads a new value from x3..x0. If "LD" is low, each FF loads its new value from its left-side neighbor. Thus, so long as "LD" is left low, the parallel-loaded value will shift rightward and output serially (LSB first) at "out." Here is a waveform diagram for the parallel-to-serial conversion of "1101" (gray means undefined).


Using negative edge-triggered flip-flops, FFs will record a new value on each falling clock edge. The waveform for parallel-to-serial conversion of " 1101 " with negative edge-triggered FFs looks exactly the same as above, except the clock must be inverted.
2. Bit-parallel even-parity generator (emits 1 iff data has an odd number of " 1 "s)
a) In the naïve implementation, the longest path between input and output (called the "critical path") passes through 5 XOR gates. If each gate has a delay of $T$, then signals propagating through the critical path incur a delay of $5 T$ between input and output. This is the so-called "worst-case delay." Note, we are ignoring wire delay.

b) For minimum delay, we can rearrange the same gates in a tree. Now, the critical path passes through only 3 XOR gates, so the worst-case delay is $3 T$.

c) In general, an $n$-input tree requires $\left\lceil\log _{2} n\right\rceil$ levels of 2 -to- 1 reduction. In this problem, each reduction is performed by a 2 -input XOR gate with delay $T$ (the same structure works with 2-input AND and OR gates). Hence the worst-case delay is $\left\lceil\log _{2} n\right\rceil T$.
3. A straightforward design for a "positive edge detector" FSM might use the following three states:

- "Zero" - most recent input was 0
- "Trans" - most recent input was 1 , transitioning from 0 (the positive edge!)
- "One" - most recent input was 1 , but not in a transition.from 0

The state transition diagram is:


The one-hot-encoded logic circuit is readily derived from the state transition diagram. Each state gives rise to one flip flop, whose input is the OR of several AND gates representing the transition arcs coming into that state. Each such AND gate computes the AND of the previous state and input value (In or In') for its corresponding transition arc. The circuit diagram follows:


Here is a waveform graph of FSM operation with input sequence " 0110 ."


