Preliminary Syllabus for EECS 150, Fall 1999

Prof. Fearing

Text: R.H. Katz, *Contemporary Logic Design*

#	Date	Lecture Topics	Reading-Katz	Lab
1	24 Aug	Boolean Alg., numbers, symbols	App.A, 5.1 Ch.1, 2:2.2	
2	26 Aug	combinational logic	2.5	
3	31 Aug	state elements	6.1	Lab 1
4	2 Sep	finite state machines	8.1, 8.2, 8.4, 8.5	Intro. to Foundation
5	7 Sep	counters, shift registers	7.1:7.3	Lab 2
6	9 Sep	FPGA Overview	10.3.4, reader	FSM
7	14 Sep	design examples	8.5, 10.4	Lab 3
8	16 Sep	timing and logic analyzer	6.1, 6.2	FPGA
9	21 Sep	busses, mux, tri-state	4.2	Lab 4
10	23 Sep	quiz review		Instrumentation
	28 Sep	QUIZ 1 (tentative)		Lab 5
11	30 Sep	wiring considerations	(Wakerly 8.4)	Shift Reg.& Counters
12	5 Oct	RAM and ROM	7.6, 4.2.5	Lab 6
13	7 Oct	serial communications		Nasty Realities
14	12 Oct	video interface, A/D		Lab 7
15	14 Oct	top-down design, synch design	7.5	SRAMS
16	19 Oct	computer data paths	11:11.2	Checkpoint 1
17	21 Oct	computer control units I	11.3	
18	26 Oct	μ programming	12.3:12.4	Checkpoint 2
19	28 Oct	computer control units, II	12:12.6	
20	2 Nov	μ programming, quiz review	5.2:5.7	Checkpoint 3
	4 Nov	QUIZ 2 (tentative)		
21	9 Nov	logic minimization, K-maps	3.1:3.3	Checkpoint 4
22	11 Nov	FSM optimization	9:9.5	
23	16 Nov	metastability, arbiter, hazards	3.4, 6.4	Checkpoint 5
24	18 Nov	testability		
25	23 Nov	error correction, handshaking	6.5	Proj. Demo deadline
26	25 Nov	Happy Thanksgiving		
27	30 Nov	HDTV		
28	2 Dec	final review		Proj. Report Due
	9 Dec	final exam		1230-330 pm