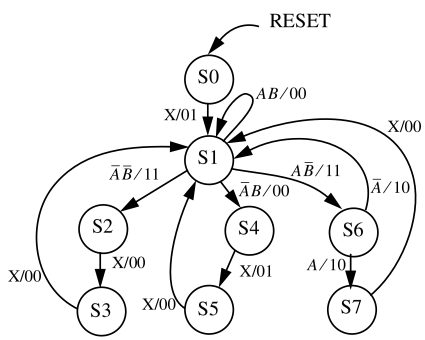
Problem 1 (16 points)

List the ROM contents in **hexadecimal** to implement the FSM shown below. The inputs A and B are synchronized. The states are assigned numerical order, e.g., for state S4, $Q_2Q_1Q_0 = 100_2$. (Follow normal state diagram assumptions: holding in the same state is implicit, etc.).

Fill in ROM contents in hexadecimal. (Binary answers will receive no credit.)

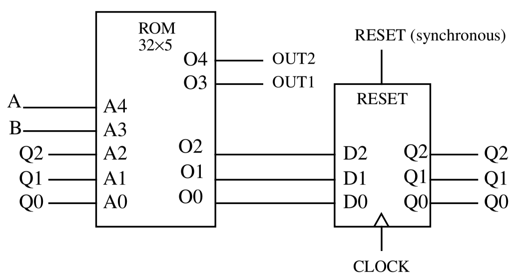
Address	**Data**	**Address**	**Data**	**Address**	**Data**	**Address**	**Data**
0		**8**		**10**		**18**	
1		**9**		**11**		**19**	
2		**A**		**12**		**1A**	
3		**B**		**13**		**1B**	
4		**C**		**14**		**1C**	
5		**D**		**15**		**1D**	
6		**E**		**16**		**1E**	
7		**F**		**17**		**1F**	



X = don't care

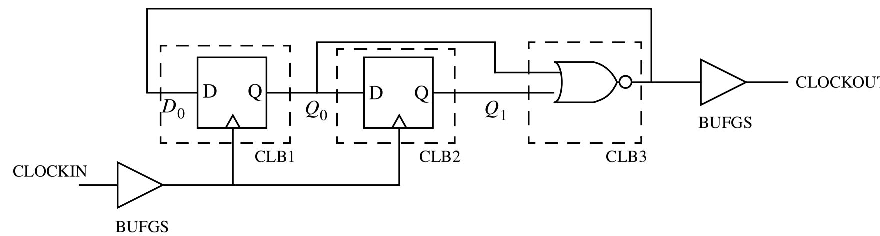
format:

AB/out2out1



Problem 2 (25 points)

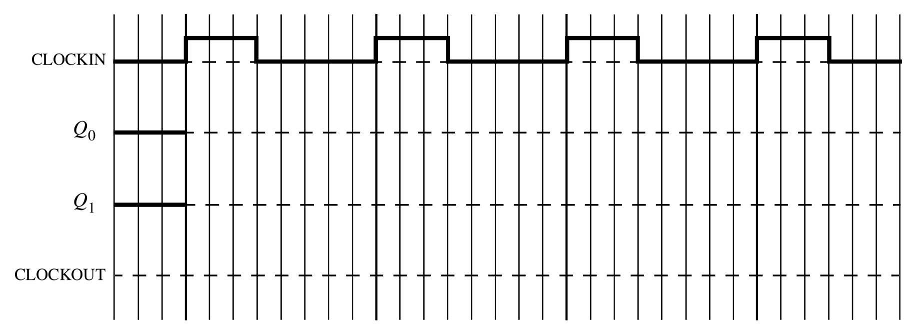
Your coworker suggests using the circuit below in a Xilinx XC4005A-4 to create a global clock signal CLOCKOUT.



[2 pts.] a) In 10 words or less, what is the intended function of this circuit? (Be as specific as possible.)

[15 pts.] b) Complete the timing diagram for this circuit using the given data. (Interconnect delay is between any CLBs.) You should exaggerate the horizontal scale as needed to show important timing details.

Parameter	Value
CLOCKIN	10 MHZ
interconnect delay	$2ns < T_{ID} < 10ns$
combinatorial delay	$T_{ILO\ max} = 4.0ns$
setup time	$T_{ICK} = 4.5ns$
hold time	0ns min
clock to output delay	$T_{CKO\ max} = 3.0ns$
clock skew	< 0.1ns



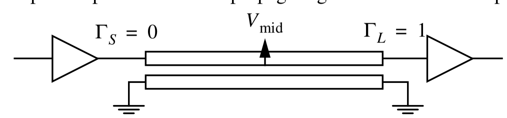
[5 pts.] **c)** Explain in 25 words or less why or why not this circuit will always function as intended.

[3 pts.] **d)** If the circuit did function correctly, what would the minimum clock period be? (Leave in algebraic form, e.g., period $\geq 2\ T_{ILO}$.)

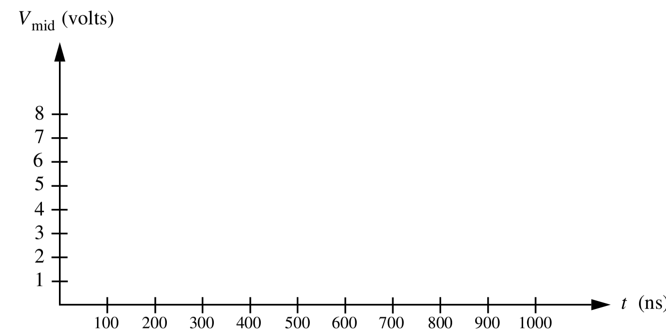
period $\geq$

Problem 3 (10 points)

A bus of length 20m with propagation velocity of $2 \times 10^8 \mathrm{ms}^{-1}$ has a driver at the transmitting end with reflection coefficient of 0 and a receiver at the opposite end with a reflection coefficient of +1. Initially, the bus is at 0V. At time $t = 0\mathrm{ns}$, a step of amplitude 2V starts propagating from transmitter output to receiver input.



Sketch V_{mid}, the voltage at the midpoint of the line, for $0 < t < 1000\mathrm{ns}$. Assume the measurement at V_{mid} has no effect on the transmission line.



Problem 4 (24 points)

Below is a data path, with 6 proposed timing diagrams shown on the next page. For each timing diagram, choose all appropriate analyses from the list below (list all possible problems). The RAM is the same as in Lab 7. Assume worst case up to 20ns timing skew on all control lines, but negligible clock skew. The clock is at 1MHz. Also assume 0ns hold time and that control signals are generated by a FSM on rising or falling edges of the same clock.

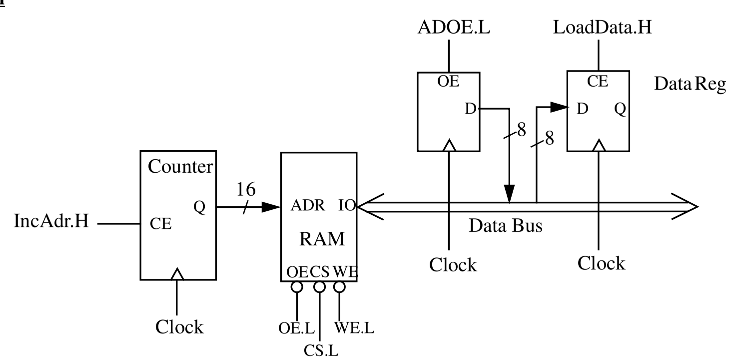
Possible analysis

a. correct timing
b. bus contention
c. data written to wrong address
d. invalid data written into RAM
e. data read from wrong address
f. invalid data read into Data Reg

Circle answer here

1.	a	b	c	d	e	f
2.	a	b	c	d	e	f
3.	a	b	c	d	e	f
4.	a	b	c	d	e	f
5.	a	b	c	d	e	f
6.	a	b	c	d	e	f

Data Path



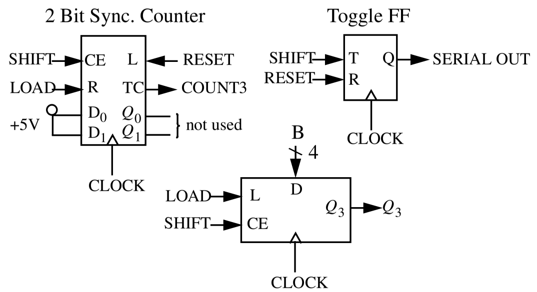
Truth Table for RAM

Mode	WE.L	CS.L	OE.L	IO Operation
Standby	**X**	**H**	**X**	**High Z**
Output disable	**H**	**L**	**H**	**High Z**
Read	**H**	**L**	**L**	D_{out}
Write	**L**	**L**	**X**	D_{in}

Problem 5 (25 points)

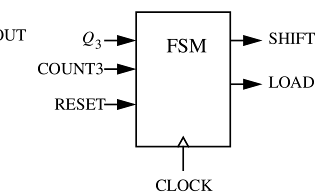
In this problem you will design the FSM controller for the serial transmitter shown below. The serial format is a variety of a **self-clocking** scheme. At the start of every bit, Serial Out changes state. A transmitted “0” is 4 clock cycles long, and a transmitted “1” is 2 clock cycles long. The transmitter loads 4 bits $B_3B_2B_1B_0$ in parallel and sends the data out MSB first. All parts have synchronous reset and load. Assume next 4 bits are ready when LOAD is asserted. $TC = 1$ when counter $Q_1Q_0 = 11$.

Data Path Block Diagram

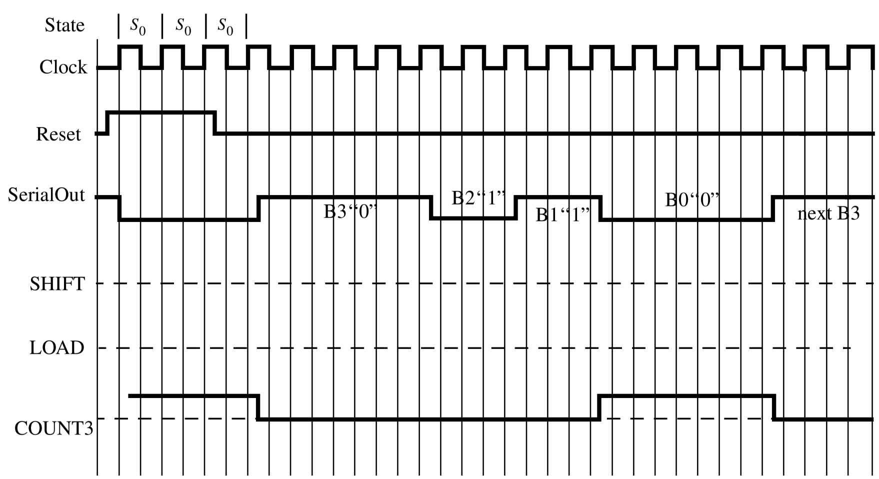


4 Bit Loadable Shift Left Register
(load has precedence over shift)

Controller Block Diagram



[15 pts.] a) Complete the timing diagram for the signals SHIFT and LOAD to get proper operation of the serial transmitter, for data $B_3B_2B_1B_0 = 0110$. Please also label states on timing diagram. Assume delays are small with respect to clock period.



[10 pts.] b) Complete the state diagram for a Mealey FSM which will generate the proper control signals for the timing diagram above and proper control of the transmitter. All transitions should be labelled explicitly in the format Q_3 COUNT3/SHIFT LOAD. Use “X” for “don’t care.