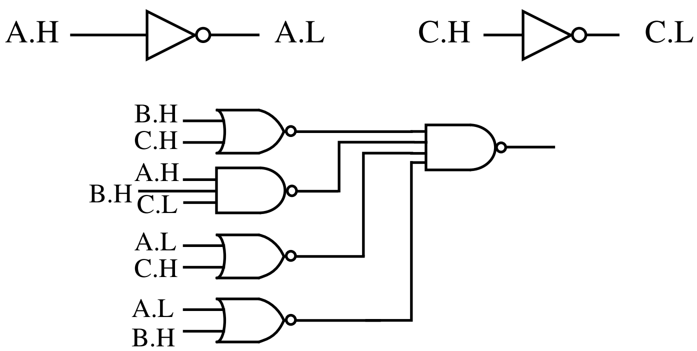
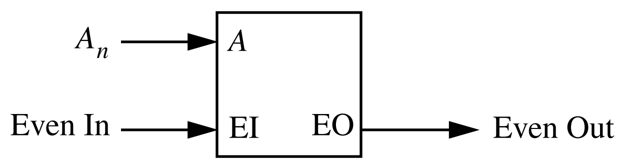
Problem 1 (25 points)

[8 pts.] **a)** You are given the logic diagram below. Complete the truth table for $Y = f(A, B, C)$. Hint: Bubble matching and simplify.



A	B	C	$Y = f(A, B, C)$
0	**0**	**0**	
0	**0**	**1**	
0	**1**	**0**	
0	**1**	**1**	
1	**0**	**0**	
1	**0**	**1**	
1	**1**	**0**	
1	**1**	**1**	

[8 pts.] **b)** In this problem you will design a combinational circuit which takes an 8 bit number A[7:0] and determines if A has an even number of ones. For example, if the input $A = 00001100_2$, then $\text{EVEN\_OUT} = 1$. The circuit is built from 1-bit modules as shown below.



Complete the truth table for the module:

A	**EI**	**EO**
0	**0**	
0	**1**	
1	**0**	
1	**1**	

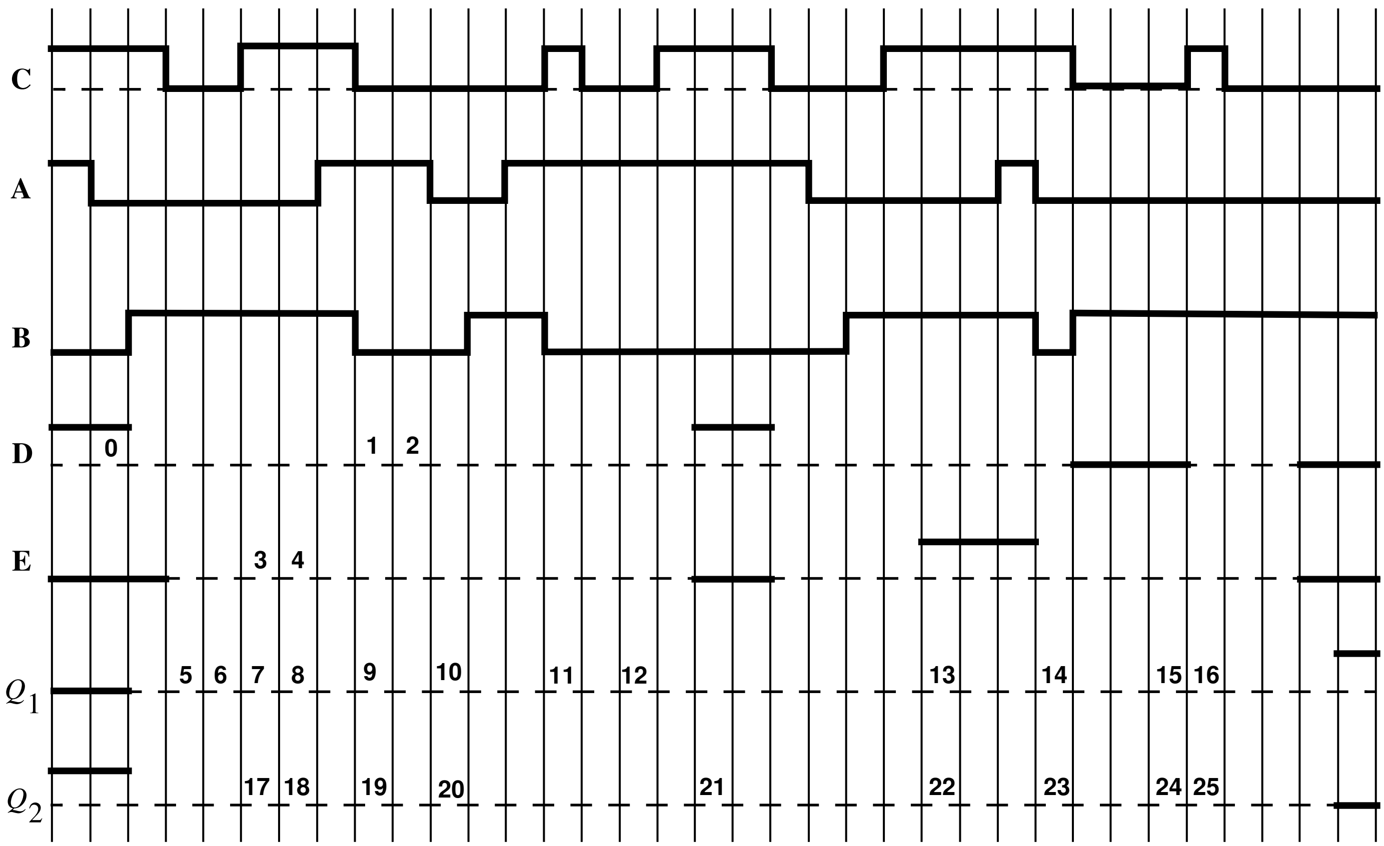
[6 pts.] **c)** Show how the 1-bit modules would be interconnected, using only wires but no extra gates or inverters, to create an 8-bit even-parity checker.

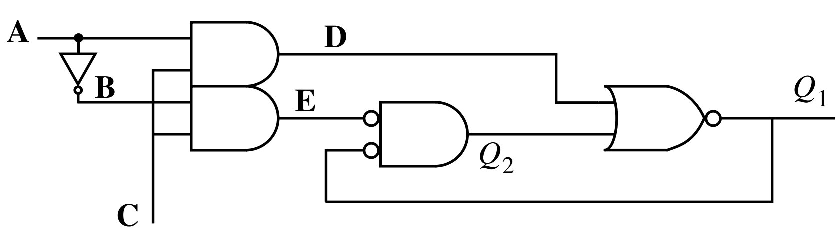
[3 pts.] **d)** Determine the maximum delay, assuming 1-unit delay for NOT/NAND/NOR, 2-unit delay for AND/OR, and 3-unit delay for XOR/XNOR.

Problem 2 (25 points) Timing

Complete the time diagram for the figure below, assuming unit delays for all gates and inverters (transport delay only), and no delay in the wires. (The dashed lines in the diagram represent missing sections of the timing diagram.) Complete the table below with the voltage levels at the specified location in the timing diagram, i.e., **L** for low and **H** for high. Example: At location 0, the appropriate *voltage* level is H. (This problem will be graded +1 for correct, 0 for blank, and −1 for incorrect, with minimum score of 0 points.)

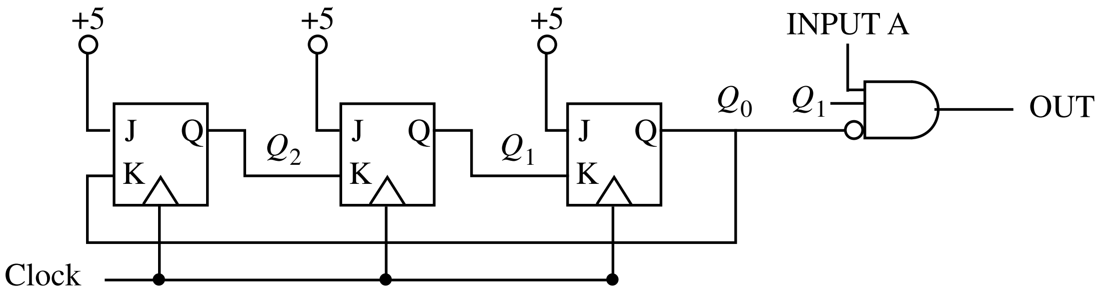
1		**6**		**11**		**16**		**21**	
2		**7**		**12**		**17**		**22**	
3		**8**		**13**		**18**		**23**	
4		**9**		**14**		**19**		**24**	
5		**10**		**15**		**20**		**25**	





Problem 3 (20 points) FSM Analysis

[12 pts.] a) You are given the following FSM to analyze. Complete the state transition table.

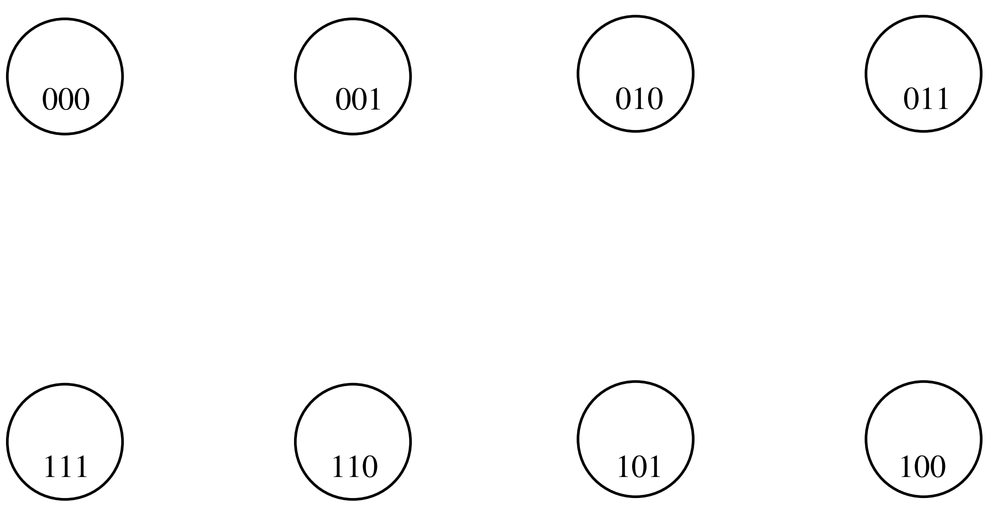


Input	**Present State**			**Next State**			**Output**
A	Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	**OUT**
0	**0**	**0**	**0**				
0	**0**	**0**	**1**				
0	**0**	**1**	**0**				
0	**0**	**1**	**1**				
0	**1**	**0**	**0**				
0	**1**	**0**	**1**				
0	**1**	**1**	**0**				
0	**1**	**1**	**1**				
1	**0**	**0**	**0**				
1	**0**	**0**	**1**				
1	**0**	**1**	**0**				
1	**0**	**1**	**1**				
1	**1**	**0**	**0**				
1	**1**	**0**	**1**				
1	**1**	**1**	**0**				
1	**1**	**1**	**1**				

[2 pts.] b) Is this a Mealey or a Moore type FSM?

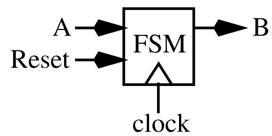
[8 pts.] **c)** You are give a state transition table for a finite state machine. Complete the state diagram below.

Input	Present State			Next State			Output
A	Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	OUT
0	**0**	**0**	**0**	**1**	**1**	**1**	**0**
0	**0**	**0**	**1**	**0**	**0**	**0**	**0**
0	**0**	**1**	**0**	**0**	**0**	**0**	**0**
0	**0**	**1**	**1**	**1**	**0**	**1**	**0**
0	**1**	**0**	**0**	**1**	**0**	**0**	**0**
0	**1**	**0**	**1**	**1**	**1**	**0**	**0**
0	**1**	**1**	**0**	**0**	**1**	**1**	**0**
0	**1**	**1**	**1**	**0**	**0**	**0**	**0**
1	**0**	**0**	**0**	**1**	**1**	**1**	**0**
1	**0**	**0**	**1**	**0**	**0**	**0**	**0**
1	**0**	**1**	**0**	**0**	**0**	**0**	**1**
1	**0**	**1**	**1**	**1**	**0**	**1**	**0**
1	**1**	**0**	**0**	**1**	**0**	**0**	**1**
1	**1**	**0**	**1**	**1**	**1**	**0**	**0**
1	**1**	**1**	**0**	**0**	**1**	**1**	**1**
1	**1**	**1**	**1**	**0**	**0**	**0**	**0**

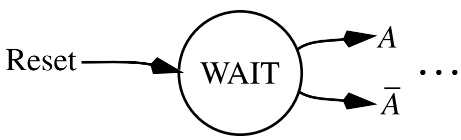


Problem 4 (20 points)

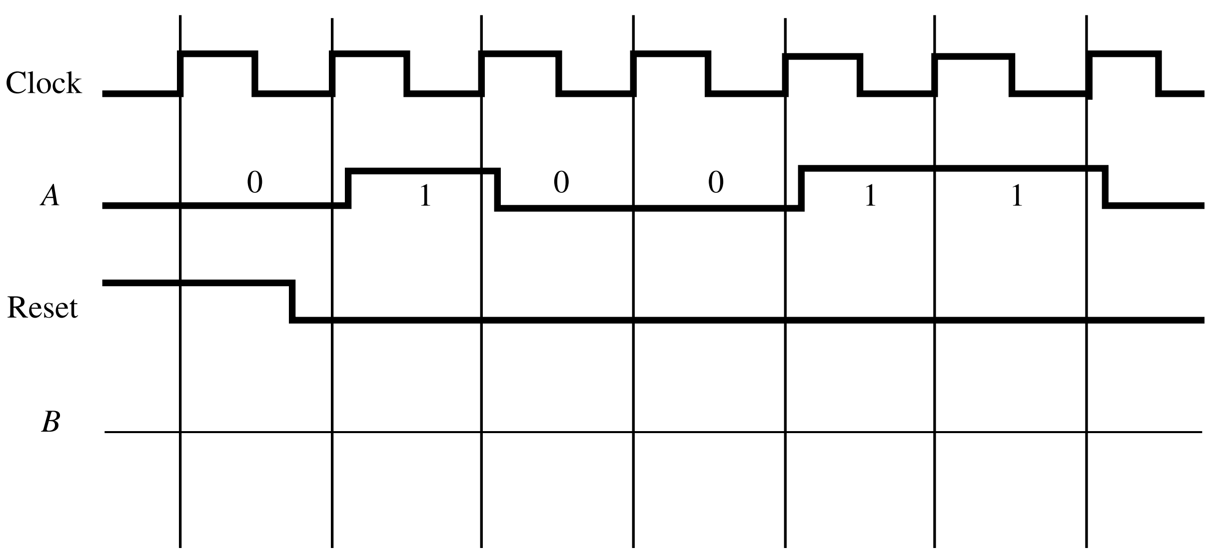
[8 pts.] a) Design a Moore FSM with synchronized input A.H, and output B.H. The FSM inputs an N digit binary number $A[N\ldots0]$ in serial form, LSB first, and outputs $B = A - 1$. For example, if $A = 110010_2$ then $B = 110001_2$. The FSM is initially in a wait state, then continually outputs bits until the FSM is reset.



Complete the state diagram for the subtract1 FSM:



[12 pts.] b) Draw a timing diagram showing B to verify your state diagram, with input $A = 110010_2$.



Problem 5 (8 points)

What is the minimum clock period for proper operation for this circuit?

minimum clock period $\boxed{}$ ns

Data:	hold time	$t_{\text{hold}} = 3\text{ns}$
	setup time	$t_{\text{setup}} = 5\text{ns}$
	propagation delay through FF	$8\text{ns} < t_{\text{cko}} < 12\text{ns}$
	propagation delay through inverter	$5\text{ns} < t_{\text{p}} < 10\text{ns}$