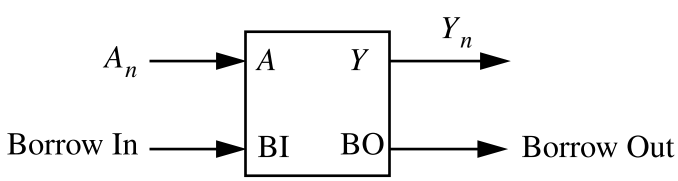
Problem 1 (25 points) Combinatorial Logic

[10 pts.] a) You are given the Boolean function $f(A, B, C) = \overline{(\overline{AB\overline{C}} \cdot \overline{BC})(\overline{\overline{A} \cdot C} \cdot \overline{\overline{A}B})}$. Complete the truth table for $f(A, B, C)$. Hint: Simplify $f(A, B, C)$.

A	B	C	$f(A, B, C)$
0	**0**	**0**	
0	**0**	**1**	
0	**1**	**0**	
0	**1**	**1**	

A	B	C	$f(A, B, C)$
1	**0**	**0**	
1	**0**	**1**	
1	**1**	**0**	
1	**1**	**1**	

[8 pts.] b) In this problem you will design a combinational circuit which takes an 8 bit number A[7:0] and calculates $Y = A - 1$. For example, if the input $A = 00001100_2$, then $Y = 00001011_2$. The circuit is built from 1 bit modules as shown below.



(1 bit module)

Complete the truth table for the module:

A	**Borrow In**	Y	**Borrow Out**
0	**0**		
0	**1**		
1	**0**		
1	**1**		

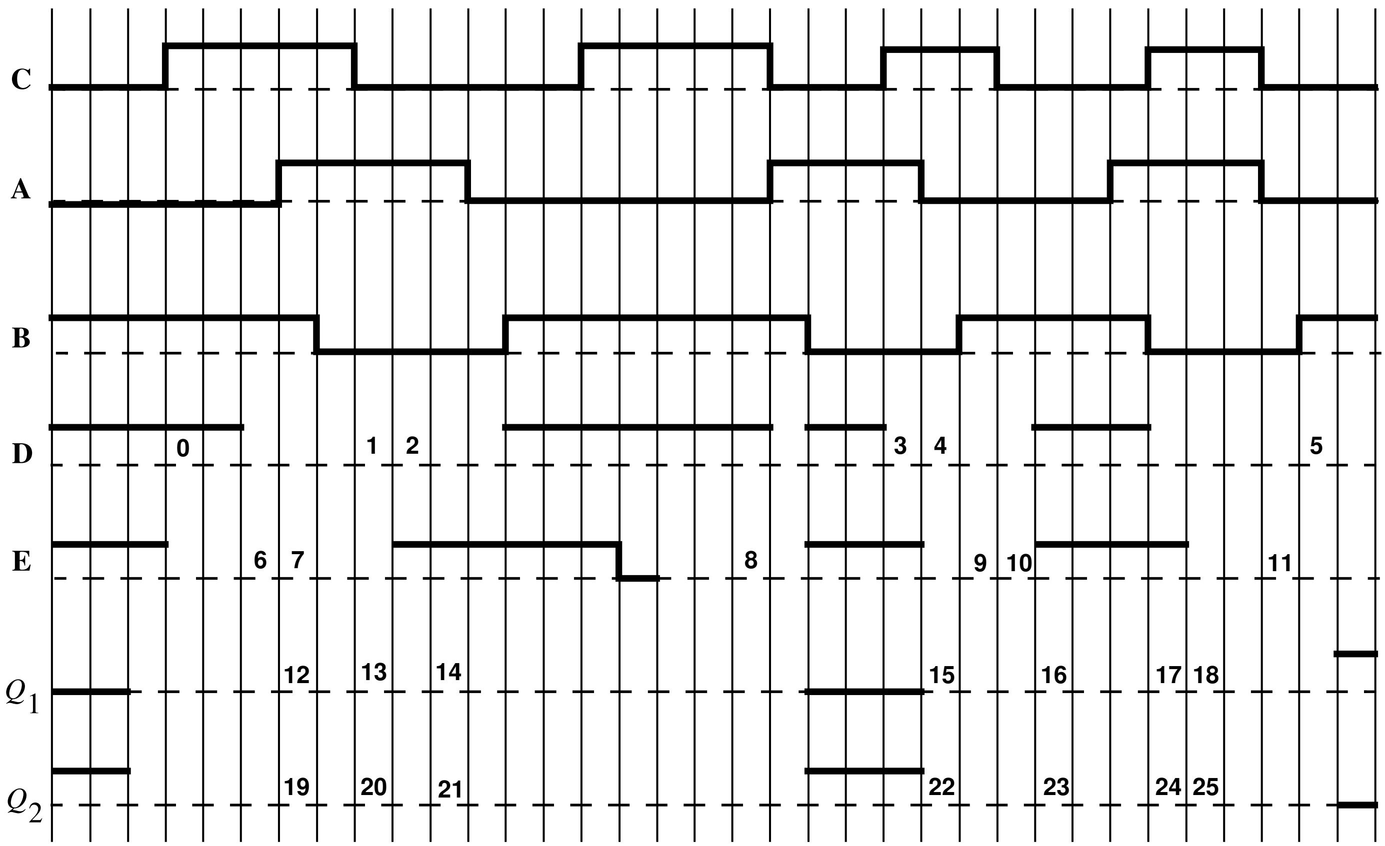
[2 pts.] c) Draw a logic diagram for functions Y and Borrow Out.

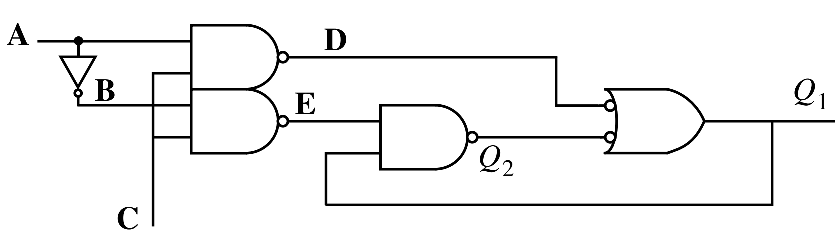
[5 pts.] d) Show how the 1-bit modules would be interconnected to create an 8-bit subtract 1 circuit.

Problem 2 (25 points) Timing

Complete the time diagram for the figure below, assuming unit delays for all gates and inverters (transport delay only), and no delay in the wires. (The dashed lines in the diagram represent missing sections of the timing diagram.) Complete the table below with the voltage levels at the specified location in the timing diagram, i.e., **L** for low and **H** for high. Example: At location 0, the appropriate *voltage* level is H. (This problem will be graded +1 for correct, 0 for blank, and −1 for incorrect, with minimum score of 0 points.)

1 _____	**6** _____	**11** _____	**16** _____	**21** _____
2 _____	**7** _____	**12** _____	**17** _____	**22**_____
3 _____	**8** _____	**13** _____	**18** _____	**23**_____
4 _____	**9** _____	**14** _____	**19** _____	**24** _____
5 _____	**10** _____	**15** _____	**20** _____	**25** _____



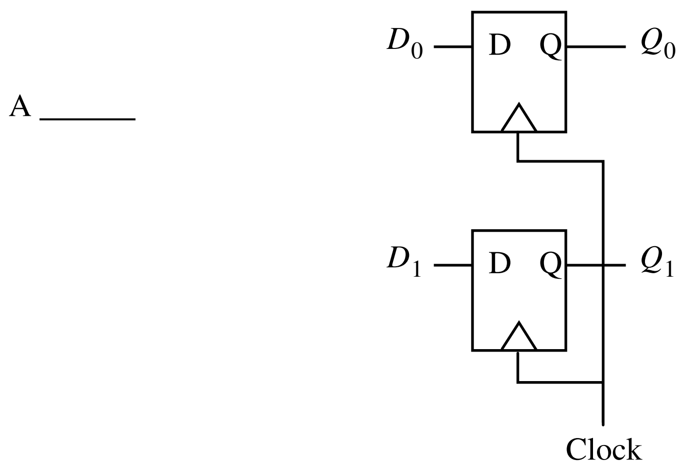


Problem 3 (20 points)

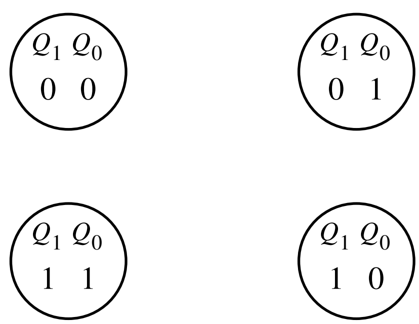
Given State Transition Table for a finite state machine (FSM).

Input	Present State		Next State	
A	Q_1	Q_0	Q_1	Q_0
0	**0**	**0**	**0**	**1**
0	**0**	**1**	**1**	**0**
0	**1**	**0**	**1**	**1**
0	**1**	**1**	**0**	**0**
1	**0**	**0**	**1**	**1**
1	**0**	**1**	**0**	**0**
1	**1**	**0**	**0**	**1**
1	**1**	**1**	**1**	**0**

[10 pts.] a) Complete the design of the FSM, using minimum number of gates, which implements the specified FSM.



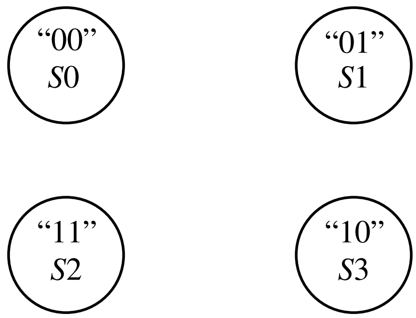
[10 pts.] b) Complete the state diagram for the FSM.



Problem 4 (20 points)

Design a Mealey FSM with synchronized input X.H and output Y.H. The output Y should be asserted for one clock cycle whenever the sequence ..011 or ..100 has been input on X. Note that patterns may be overlapping, e.g., X = ..0000111000.. generates Y = ..000001001.. . (The patterns may also overlap themselves.) The machine should start assuming that a “0” has already been input.

[12 pts.] a) Complete the state diagram for the sequence detector:



[8 pts.] b) Complete the state table for the FSM.

Input X.H	**Current State** Q_1Q_0	**Next State** Q_1Q_0	**Output Y.H**
0	$S0$		
1			
0	$S1$		
1			
0	$S2$		
1			
0	$S3$		
1			

Problem 5 (10 points)

What is the minimum clock period for proper operation for this shift register circuit?

minimum clock period [ns]

Data: hold time $t_{hold} = 6ns$

setup time $t_{setup} = 20ns$

propagation delay through FF $8ns < t_{cko} < 12ns$