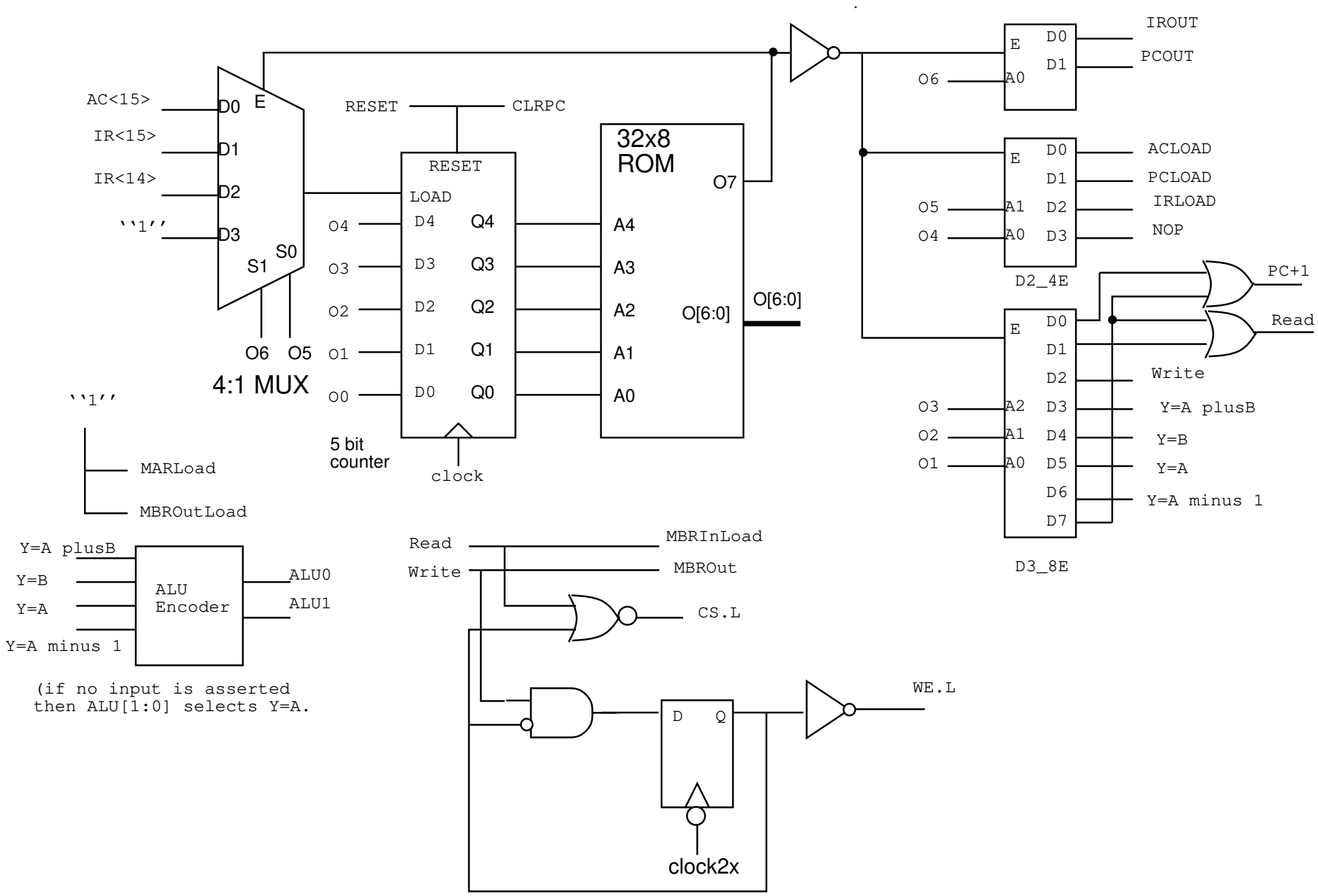
AC<15>
IR<15>
IR<14>
''1''
D0
D1
D2
D3
E
S0
S1
O6
O5
4:1 MUX
RESET
CLRPC
RESET
LOAD
O4
O3
O2
O1
O0
D4
D3
D2
D1
D0
Q4
Q3
Q2
Q1
Q0
5 bit
counter
clock
32x8
ROM
O7
A4
A3
A2
A1
A0
O[6:0]
O[6:0]
IROUT
PCOUT
O6
E
D0
D1
A0
ACLOAD
PCLOAD
IRLOAD
NOP
O5
O4
A1
A0
D2
D3
D2_4E
PC+1
Read
Write
Y=A plusB
Y=B
Y=A
Y=A minus 1
O3
O2
O1
A2
A1
A0
D3
D4
D5
D6
D7
D3_8E
''1''
MARLoad
MBROutLoad
Y=A plusB
Y=B
Y=A
Y=A minus 1
ALU
Encoder
ALU0
ALU1
(if no input is asserted
then ALU[1:0] selects Y=A.
Read
Write
MBRInLoad
MBROut
CS.L
WE.L
D
Q
clock2x