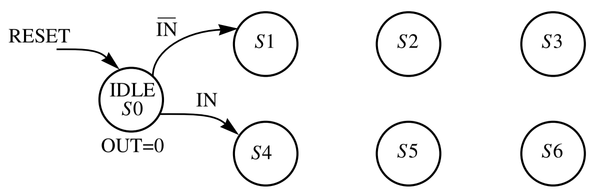
## Problem 1 FSM Design Problem (15 points)

1. In this problem, you will design an FSM which takes a synchronized serial input IN (presented LSB first) and outputs a serial bit stream OUT which represents the input plus 3. For example, if the input were $1010_2$ the output stream would be $1101_2$. (Note that there is an output bit for every input bit. In the idle state on RESET, a zero is output.) Hint: the state machine needs to keep track of the carry bit.

**[8 pts.]** **a)** Complete the state diagram for a Moore type FSM. Be sure to specify labels on transitions, and outputs.




**[7 pts.]** **b)** Complete the state table for the Moore FSM which implements the plus 3 function.

| Input IN | Present State | Next State | Output OUT |
|---|---|---|---|
| 0<br>1 | S0 | | |
| 0<br>1 | S1 | | |
| 0<br>1 | S2 | | |
| 0<br>1 | S3 | | |
| 0<br>1 | S4 | | |
| 0<br>1 | S5 | | |
| 0<br>1 | S6 | | |



## Problem 2 FSM Design Problem (10 points)

Design a Moore FSM which outputs a single high pulse of width one clock cycle every time the synchronized input signal START changes from 0 to 1.

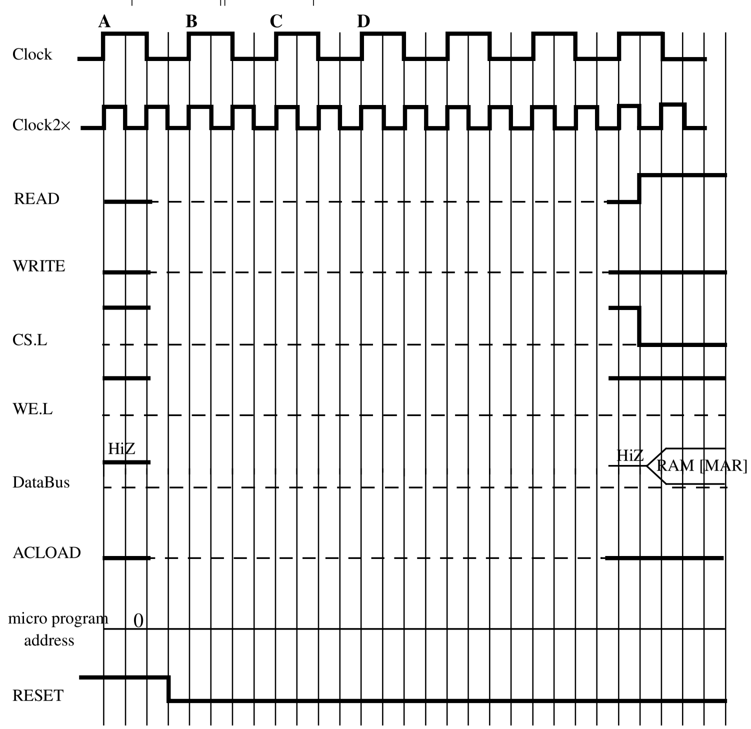
**[7 pts.]** **a)** Show state diagram:

**[3 pts.]** **b)** Show schematic for this FSM using type D FF(s) and minimal extra gates.

## Problem 3 FSM/Microprogram Analysis (20 points)

**[12 pts.] a)** Complete the timing diagram for the computer data path and control unit shown on the next page. All components are synchronous. The microprogram ROM contents in Hexadecimal are:

| Address | Hex Data | Address | Hex Data |
|---|---|---|---|
| 0 | 38 | 4 | EO |
| 1 | 32 | 5 | EO |
| 2 | 06 | 6 | EO |
| 3 | 34 | 7 | EO |




**[2 pts.] b)** Label the timing diagram with the micro program address.

**[6 pts.] c)** List, in register transfer notation, the data transfer occurring at and after the noted clock edge.

A: $0 \rightarrow PC$, $0 \rightarrow \mu PC$ B: ____________________

C: ____________________ D: ____________________

## Problem 4 Microprogramming (10 points)

Write a microprogram, in symbolic form, to execute a new instruction for the computer shown on page 4. The new instruction is “decrement accumulator and branch if greater than or equal to zero” DBGE address.

The instruction format is

| 15 | | 0 |
|---|---|---|
| 1 | 1 | branch address |

Assume the instruction has already been fetched and is loaded into IR.

You have two micro-instructions available, DO and JMP.

| Label | Operation | Comment |
|---|---|---|
| **DBGE** | | |
| **DONE** | **JMP (always) FETCH** | **get next instruction from RAM** |

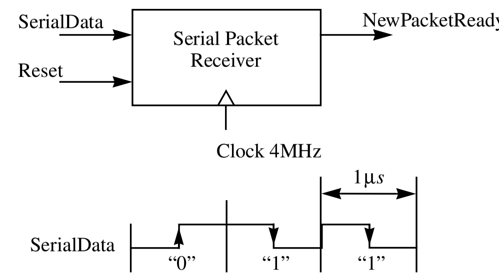


## Problem 5 Top Down Design (25 points)

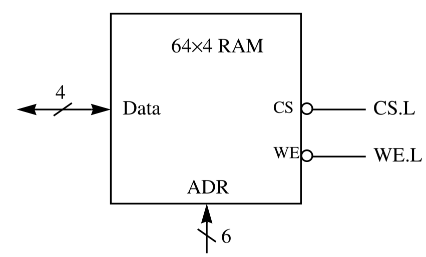
In this problem you will design the data path for a serial packet receiver. (A packet is a group of bits.) The serial packet receiver receives 256 data bits and stores them in a 64×4 RAM. After 256 bits have been received and the RAM is full, the system asserts NewPacketReady and halts until the next Reset is asserted.

The unsynchronized SerialData input uses a code 01 to represents a “0” data bit and a code 10 to represent a “1” data bit. The code words are presented LSB first at a rate of 1 MHz. The internal clock of the system is 4 MHz. (Thus, on average there are 4 internal clocks per input data bit, and 2 internal clocks per input code bit.)

A basic block diagram of the system is shown here:



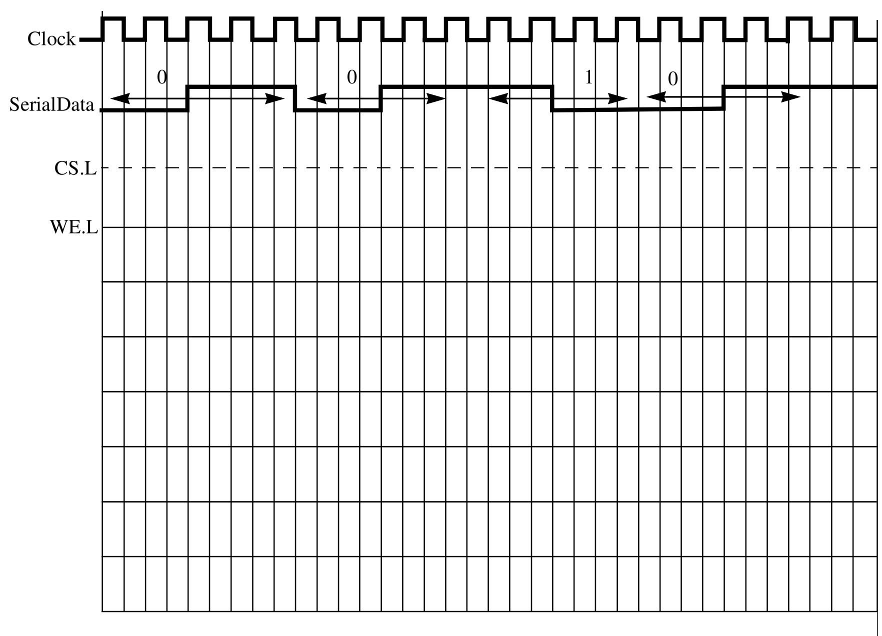

**[10 pts.] a)** Draw a detailed block diagram of a data path which could be used to decode the input SerialData and fill the RAM with the data. Your block diagram should be to the level of building blocks such as MUXes, registers, counters, shift registers, decoders, etc.



**[5 pts.] b)** List signals which come from the data path and are input to the controller:

List control signals generated by the controlled which control the data path.

**[10 pts.] c)** Draw a timing diagram which shows all the relevant control signals necessary for reading in the first 4 code words, storing in RAM, and updating the RAM address. Assume that control signals are generated by a Moore type FSM running at 4 MHz. Show as many signals as necessary. Assume the system has already received 16 bits.






## Problem 6 Short Answer Section (20 points)

**[2 pts.] a)** Can metastability be completely eliminated in real digital systems with external inputs? If yes, how can metastability be eliminated? If no, what can be done to minimize problems?

**[2 pts.] b)** You observe that an FSM with 100ns clock period and 1MHz asynchronous input (which is synchronized by a D type-edge triggered FF) fails to go to the correct next state on average once per second. The Xilinx timing analyzer tells you that the minimum clock period is 97 ns for the circuit. When you change the clock period to 110 ns, the error disappears. What is a possible cause for the FSM faulty next state?

**[2 pts.] c)** You have been asked to design a certain digital system for a portable multimedia application. The marketing department tells you to make a case for using either digital hardware or a general purpose CPU and software to implement certain algorithms.

List 3 reasons why the digital hardware (e.g., Xilinx or custom VLSI chip) approach might be better:

1)

2)

3)

List 3 reasons why the general purpose CPU and software approach might be better:

1)

2)

3)

**[1 pts.] d)** Explain what a tri-state device is (what are the three states)? When are tristate devices useful?

**[3 pts.] e)** Find the minimal sum-of-products form for $Y = \bar{A}\bar{C}\bar{D} + \bar{A}\bar{B}C + \bar{B}\bar{C}D + A\bar{B}D + \bar{A}BC\bar{D}$.

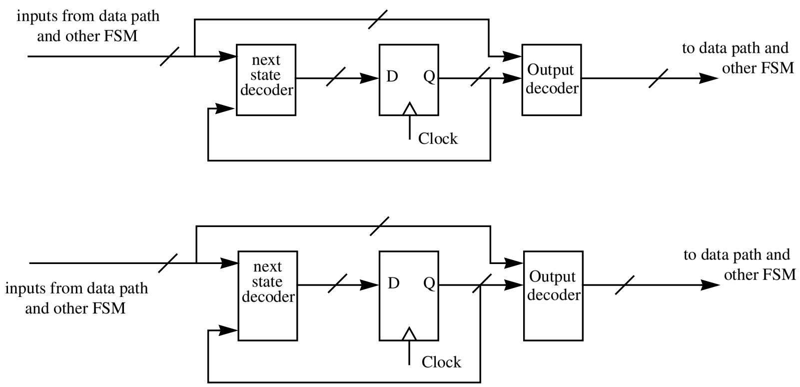
**[2 pts.] f)** A system has two Xilinx boards. On each board, the output of the Xilinx chip is clean, when you connect these outputs through a 0.5m cable to another Xilinx board, now there are glitches on the signal and clock lines. Suggest a likely cause of the glitches.

**[3 pts.]** **g)** You are working with a Xilinx board which works perfectly with theTA .bit file. Your design simulates without a problem using ViewSim. Your .bit file configures the Xilinx correctly, but your design does not function.

1) What is the most likely cause of the problem?

2) Suggest a plan for finding, then fixing the problem?

**[2 pts.]** **h)** A student project has two communicating Mealey machines connected, as shown below. What is the biggest potential problem with this design? Show how by simply changing some connections the problem will go away.




**[3 pts.]** **i)** State minimization. For the following state table, determine which states are equivalent.

| **Present state** | **INPUT** | **Output** | **Next state** |
|---|---|---|---|
| S0 | 0 | 1 | S1 |
| S0 | 1 | 1 | S3 |
| S1 | 0 | 0 | S2 |
| S1 | 1 | 0 | S0 |
| S2 | 0 | 1 | S3 |
| S2 | 1 | 1 | S1 |
| S3 | 0 | 0 | S0 |
| S3 | 1 | 0 | S2 |