UNIVERSITY OF CALIFORNIA

College of Engineering
Department of Electrical Engineering
and Computer Sciences

Professor Fearing

Fall 1999

EECS 150 – QUIZ #2

Tuesday, 4 November 1998, 2:10-3:30 p.m.

Name: ___________________________________ ID#: _____________

- Closed book. No notes. No calculators.
- There are 4 problems worth 100 points total. There is little room for partial credit—it's better to do half the test carefully than to do the entire test sloppily.

Problem	Points	Your Score
1	16	
2	20	
3	50	
4	14	
Total	100	

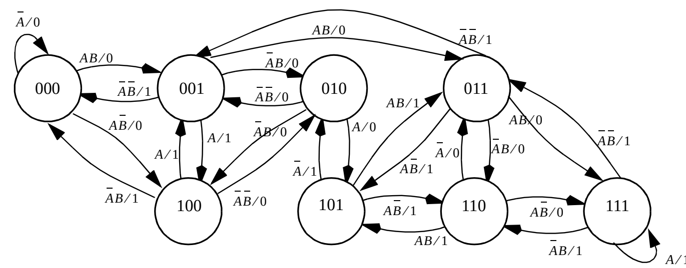
In the real world, unethical actions by engineers can cost money, careers, and lives. The penalty for unethical actions on this exam will be a grade of zero.

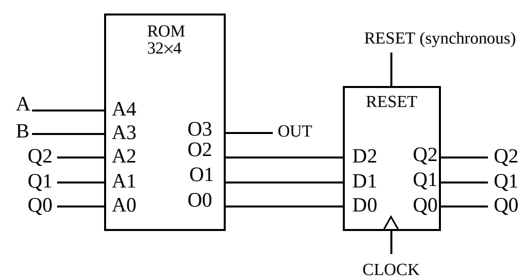
Problem 1 (16 points)

List the ROM contents in **hexadecimal** to implement the FSM shown below. The inputs A and B are synchronized. The states are assigned numerical order, e.g., for state S4, $Q_2Q_1Q_0 = 100_2$. (Follow normal state diagram assumptions: holding in the same state is implicit, etc.).

Fill in ROM contents in hexadecimal. (Binary answers will receive no credit.)

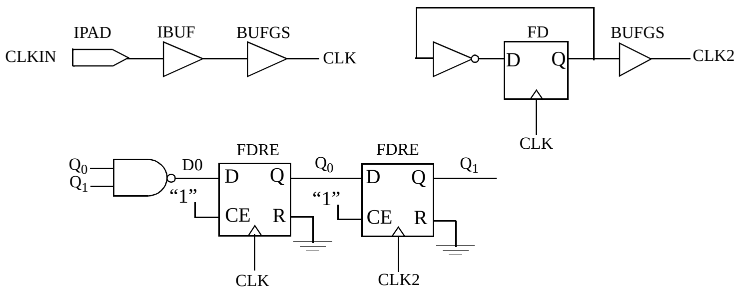
Address	Data	Address	Data	Address	Data	Address	Data
0		**8**		**10**		**18**	
1		**9**		**11**		**19**	
2		**A**		**12**		**1A**	
3		**B**		**13**		**1B**	
4		**C**		**14**		**1C**	
5		**D**		**15**		**1D**	
6		**E**		**16**		**1E**	
7		**F**		**17**		**1F**	



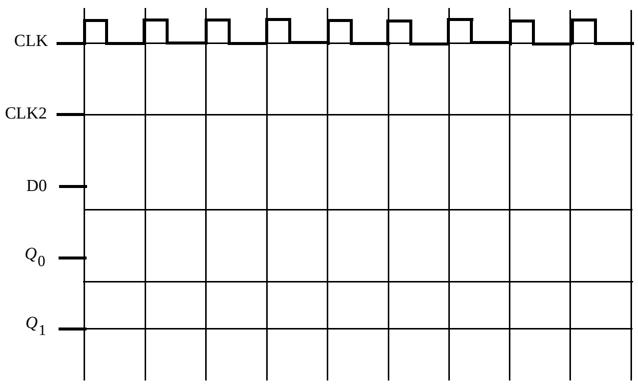


Problem 2 (20 points)

Your lab partner has designed the following Xilinx XC4000 circuit and tells you it works fine in unit delay simulation, but won't work when downloaded to the Xilinx chip. Given CLKIN=1MHz, T_{ckomax}=2.8ns, T_{su}=2.4ns.



[12 pts.] a) Complete the timing diagram (considering propagation and interconnect delays) to show why the circuit does not operate as intended.



[4 pts.] b) Circle the problem area(s) in the timing diagram, and briefly explain in a full sentence what the problem is.

[4 pts.] c) Modify the design above so it will work as intended. Do not add any gates or FF.

Problem 3 (50 points)

You are given the 8-bit data path below. The SRAM is 256×8, but has the same operating characteristics as the static RAM used in lab. 8-bit binary counter CB8RE has synchronous reset.