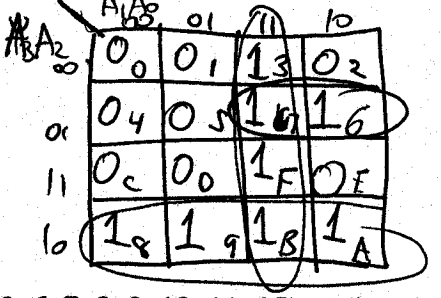
KEY Fall 1999 Final $\bar{x} = 55/83.5$ $\sigma = 17.7$

Problem 1 (14 points)

[4 pts.] **a)** Find the minimal sum-of-products form for $Y = \sum(3, 6, 7, 8, 9, 10, 11, 15)$ using variables $A_3A_2A_1A_0$. (For example, minterm 3 = $\bar{A}_3\bar{A}_2A_1A_0$.)

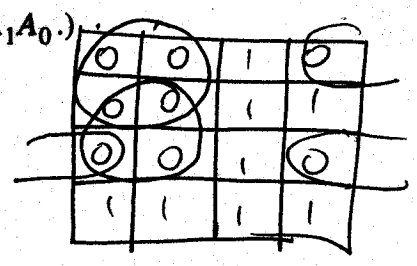
$Y = A_1A_0 + A_3\bar{A}_2 + \bar{A}_3A_2A_1$



[4 pts.] **b)** Find the minimal product-of-sums form for $Y = \sum(3, 6, 7, 8, 9, 10, 11, 15)$ using variables $A_3A_2A_1A_0$. (For example, For example, minterm 3 = $\bar{A}_3\bar{A}_2A_1A_0$.)

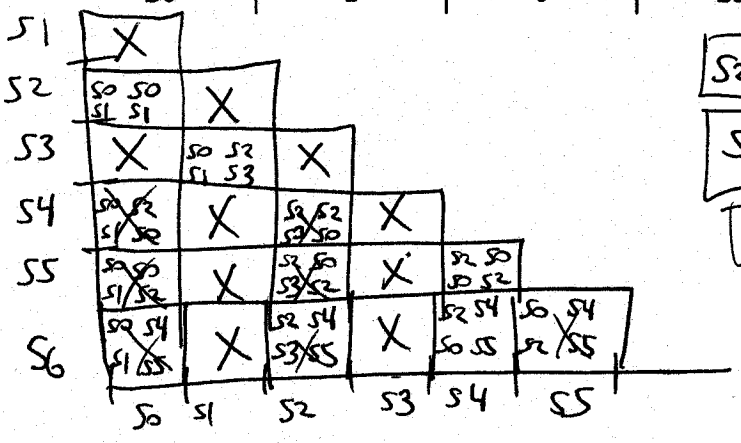
$Y = \bar{A}_3 \cdot \bar{A}_1 + A_2 \cdot \bar{A}_1 + \bar{A}_3\bar{A}_2\bar{A}_0 + A_3A_2\bar{A}_0$

$Y = (A_3 + A_1)(\bar{A}_2 + A_1)(A_3 + A_2 + A_0)(\bar{A}_3 + \bar{A}_2 + A_0)$



[6 pts.] **c)** *State minimization.* For the following state table, determine which states are equivalent.

Present State	Input	Output	Next State
S0	0	0	S0
S0	1	0	S1
S1	0	1	S0
S1	1	1	S1
S2	0	0	S2
S2	1	0	S3
S3	0	1	S2
S3	1	1	S3
S4	0	0	S2
S4	1	0	S0
S5	0	0	S0
S5	1	0	S2
S6	0	0	S4
S6	1	0	S5



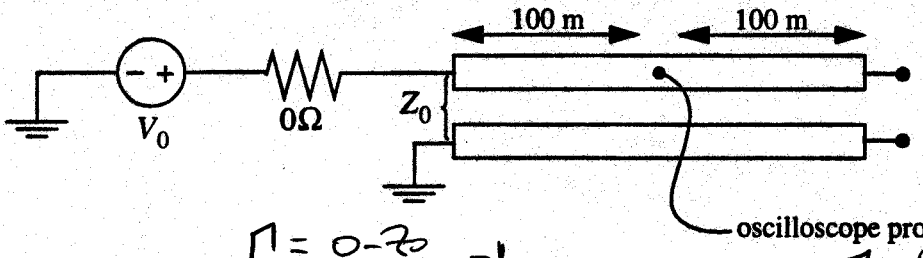
$S_2 = S_0$

$S_1 = S_3$

$S_4 = S_5$

Problem 2 (6 points) KEY

You are given a 200-meter length of cable with impedance 50 ohms and propagation velocity 2×10^8 m/s. The source end is driven with a 0-ohm impedance. The load end is open circuited. An oscilloscope probe (with 10-meg ohm input impedance) is connected to the cable 100 meters from the source, as shown below:

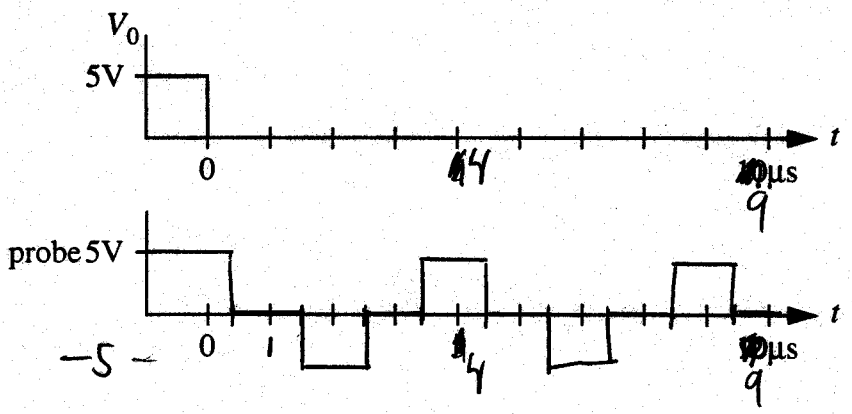


$t = \frac{d}{v} = \frac{10^2}{2\times10^8} = 0.5\mu s$

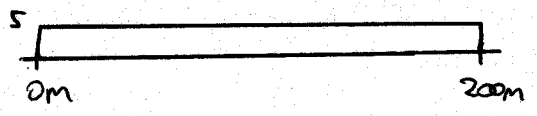
$\Gamma = \frac{0-Z_0}{0+Z_0} = -1$

$\Gamma = \frac{\infty-Z_0}{\infty+Z_0} = +1$

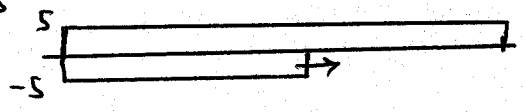
V_0 switches at time $t = 0$, as shown. Sketch the voltage seen on the oscilloscope for $0 < t < 10\mu s$. (V_0 is initially at 5V, $-\infty < t < 0$.)



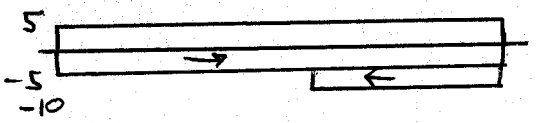
$t=0^-$



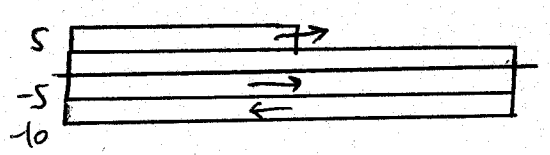
$t=0.5\mu s$



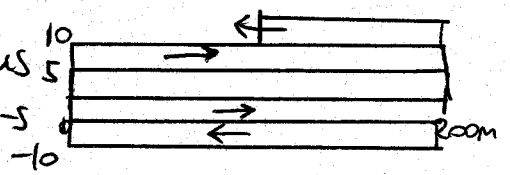
$t=1.5\mu s$



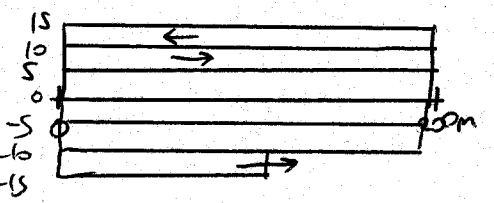
$t=2.5\mu s$



$t=3.5\mu s$

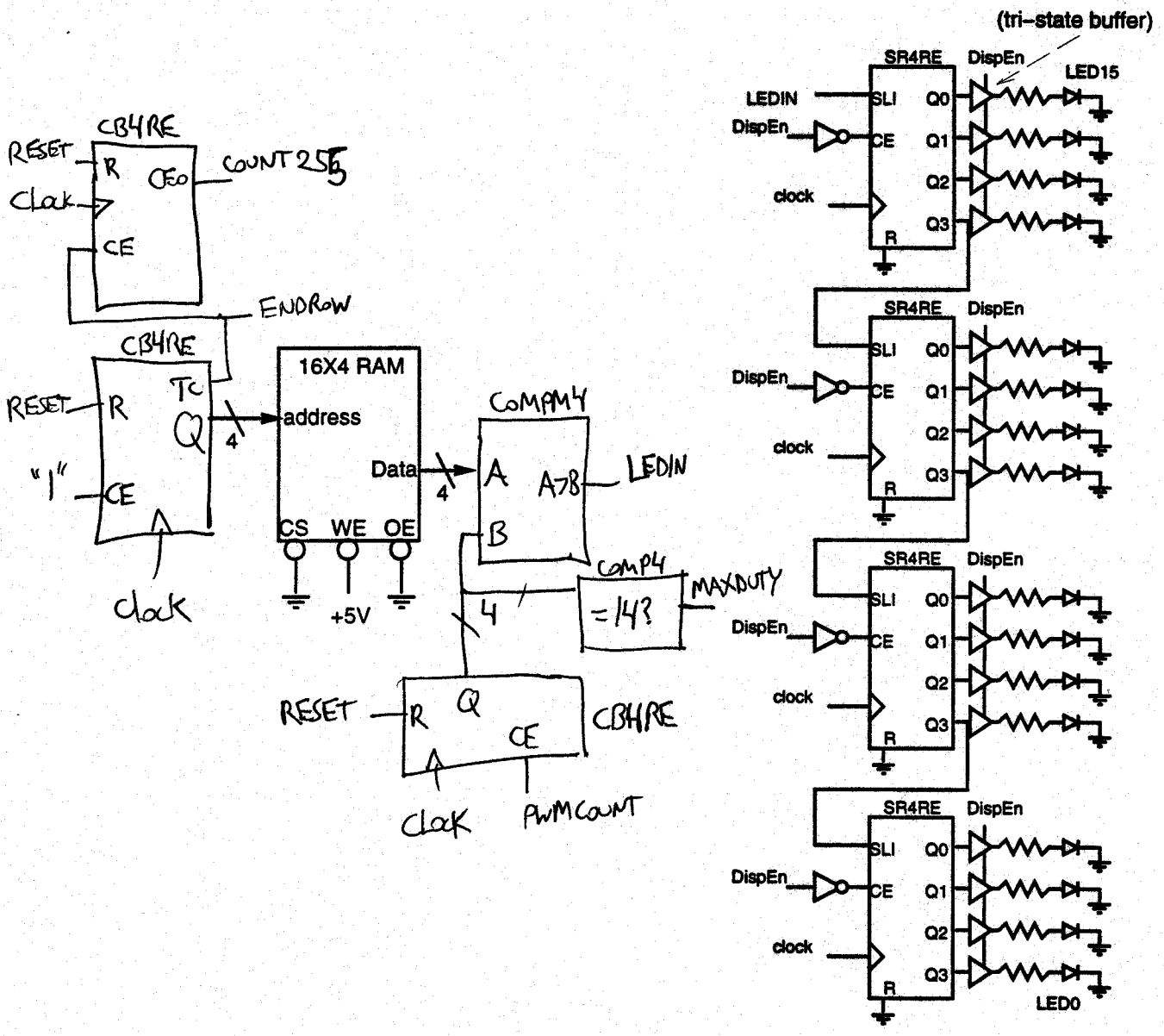


$t=4.5\mu s$



Problem 3 Serial LED PWM Display (25 points)

In this problem, you will design the data path and controller state diagram for a 16-element LED display. The brightness of each LED is controlled by its duty cycle (using pulse width modulation), which is specified by a 4-bit value (0/15, 1/15, 2/15, ... , 15/15) stored in a 16×4 RAM. All components are driven by a 10MHz system clock. The data (on/off for each LED) is shifted into the display shift register in 1.6µs, then displayed for 24.0µs.



[11 pts.] a) Complete a detailed block diagram of the data path for the LED PWM Display, using up to three CB4RE synchronous binary counters, one COMPM4 4-bit magnitude comparator, and one COMP4 identity comparator. Note that CB4RE has both a TC output = $Q_3 \cdot Q_2 \cdot Q_1 \cdot Q_0$ and CEO = $TC \cdot CE$. Also, SR4RE shifts left.

Problem 3 (cont.)

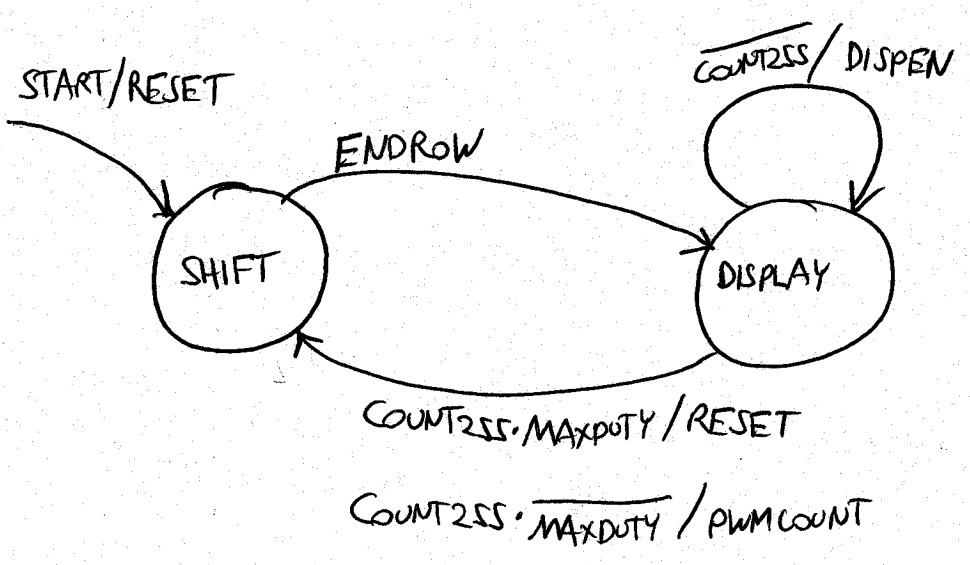
[1 pts.] b) List the input signals to the data path that come from the control FSM.

RESET
PWMCOUNT
DISPEN

[1 pts.] c) List the output signals from the data path that are inputs to the control FSM.

MAXDUTY
ENDROW
COUNT255

[10 pts.] d) Draw (a) state diagram(s) for a control FSM that will continuously turn on each LED for a fraction of time proportional to the value of its corresponding RAM location. (For example, if address 3 has contents 8, then LED3 should be on 8/15 of the display enable time.) Do not use more than 3 states. Ensure that FSM and data path start correctly.



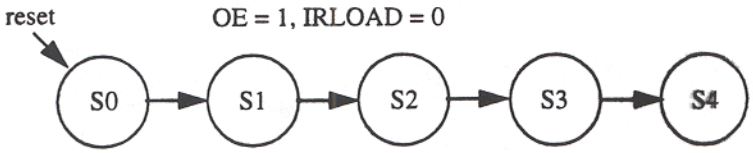
Note: PWM COUNT goes 0... 14, so that data = 0 is off (A>B=0) and data = 15$_0$ is on fully (A>B=1 for A=15, B≤14).

[2 pts.] e) Why does the clock to the shift register need to be as fast as possible?

So that the LEDs can be enabled for as long as possible to increase brightness and brightness range.

Problem 4 (cont.) – Data paths

a.



IROUT↑ | IROUT↑ RBUSOUT WE↓ CS↓ | IROUT↑ RBUSOUT | MBRLOAD CS↓

clock edge 1: NOP

clock edge 1.5: NOP

clock edge 2: MBR→RAM[IR]

clock edge 2.5: MBR→RAM[IR]

clock edge 3: NOP

clock edge 4: RAM[IR]→MBR

Bold

Vers #1 | Vers #2

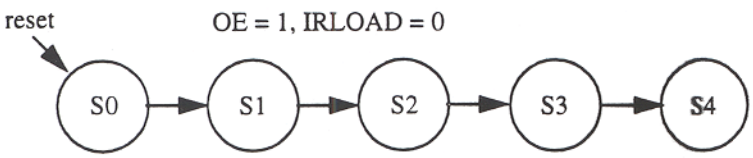
timing diagram (from page 9) ☐ B | A

Are bus conflicts possible? yes

If yes, state ~~where~~ when they occur:

edge 1.5, 2.5 RAM reading + MBROUT

b.



IROUT RBUSOUT↑ WE↑ | IROUT CS | MBRLOAD IROUT CS

timing diagram (from page 9) ☐ A | B

Are bus conflicts possible? yes

If yes, state where they occur:

edge 3, edge 2

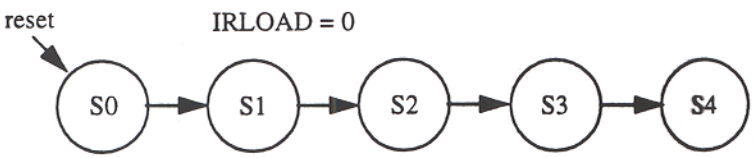
clock edge 1: NOP

clock edge 2: NOP ← possible garbage writes

clock edge 3: MBR→RAM[IR] ←

clock edge 4: RAM[IR]→MBR

c.



IROUT↑ | IROUT↑ WE↓ CS | IROUT↑ RBUSOUT CS | MBRLOAD OE CS

clock edge 1: NOP

clock edge 1.5: NOP

clock edge 2: MBR→RAM[IR]

clock edge 2.5: MBR→RAM[IR]

clock edge 3: NOP

clock edge 4: RAM[IR]→MBR

timing diagram (from page 9) ☐ D | C

Are bus conflicts possible? yes

If yes, state where they occur:

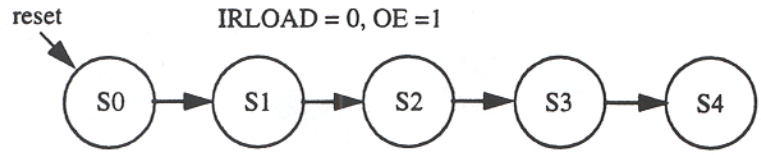
~~between 2.5 & 3~~

↑ 1, 3, 4 (+ε)

(OE, RBUSOUT, CS) simultaneous

Problem 4 – Data paths (cont.)

d.



Bold

IROUT↑ WE↑ | IROUT↑ CS↓ WE↑ RBUSOUT↑ | IROUT↑ | CS↓ MBRLOAD

timing diagram (from page 9) ☐ G / H

clock edge 1: NOP

clock edge 1.5: Nop

clock edge 2: Hiz → RAM[IR]

clock edge 2.5: MBR→RAM[IR]

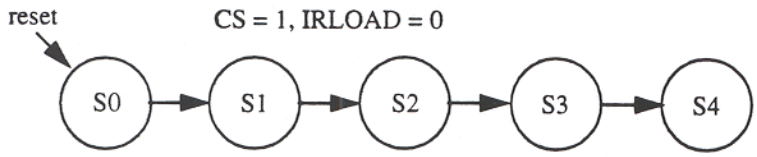
clock edge 3: NOP

clock edge 4: RAM[IR] → MBR

Are bus conflicts possible? No

If yes, state where they occur:

e.



WE↓ IROUT | RBUSOUT IROUT | MBRLOAD OE IROUT

timing diagram (from page 9) ☐ E / F

clock edge 1: NOP

clock edge 1.5: NOP

clock edge 2: Hiz →RAM[~~IR~~MBR]

clock edge 2.5: MBR→RAM[IR]

clock edge 3: NOP

clock edge 4: RAM[IR]→MBR

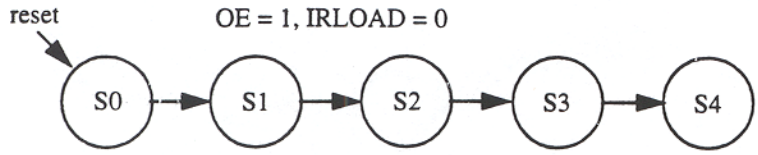
Are bus conflicts possible? yes

If yes, state where they occur:

edge 3, 1, 4

(OE, RBUSOUT glitchy)

f.



IROUT↑ | WE↑ CS↓ IROUT↑ | RBUSOUT IROUT↑ | MBRLOAD CS↓

timing diagram (from page 9) ☐ C / D

clock edge 1: NOP

clock edge 1.5: NOP

clock edge 2: NOP

clock edge 2.5: MBR→RAM[IR]

clock edge 3: NOP

clock edge 4: RAM[IR] → MBR

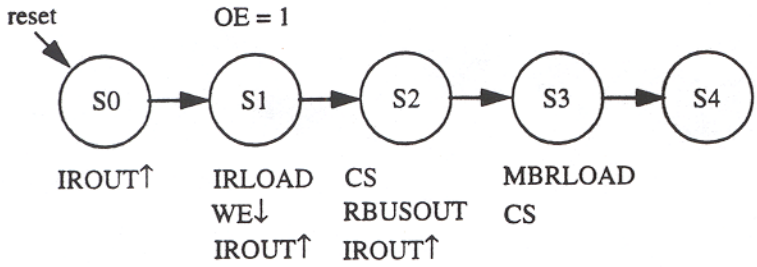
Are bus conflicts possible? yes

If yes, state where they occur:

edge 2, edge 4

Problem 4 – Data paths (cont.)

g.



Bld

timing diagram (from page 9) ☐ H / G

clock edge 1: NOP

clock edge 1.5: NOP

clock edge 2: Hi-Z → IR

clock edge 2.5: MBR → RAM[IR] (random location)

clock edge 3: NOP

clock edge 4: RAM[IR] → MBR

Are bus conflicts possible?

yes

If yes, state where they occur:

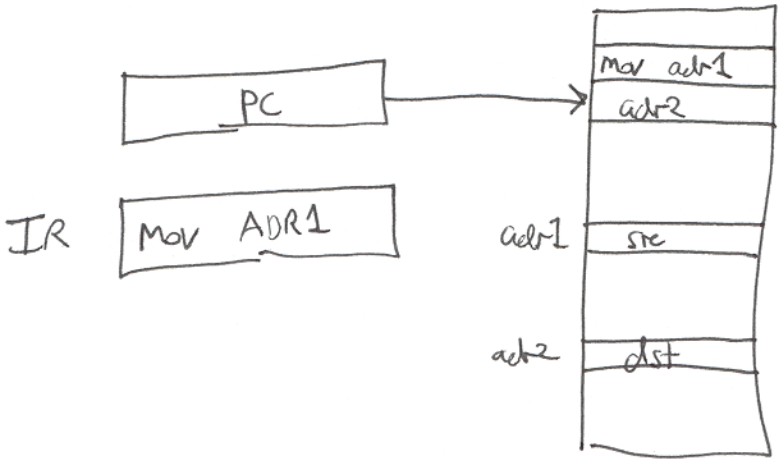
1+ε between 2.5+3.0, 4+ε (since RBUSOUT + CS can have glitches)

Problem 5 (15 points)

[12 pts.] a) Using the data path on page 11 and microprogrammed controller on page 12, write a microprogram, in symbolic form, to execute the following register transfer operations in the order listed:

RTN	Microcode
1) RAM[IR] → MBR	Do IROUT/NOP/NOP/NOMBR (setup IROUT) Do PCOUT/NOP/READ/MBRLOAD
2) RAM[PC] → IR	Do IROUT/IRLOAD/READ/NOMBR (uses PC adr)
3) MBR → RAM[IR]	Do IROUT/NOP/WRITE0 Do IROUT/NOP/WRITE1
4) PC+1 → PC	Do IROUT/NOP/PC+1/NO MBR

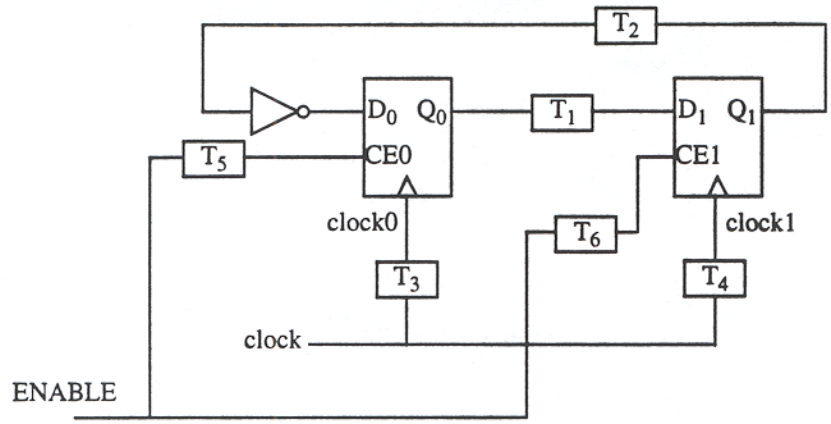
[3 pts.] b) Assuming the RTN in part (a) represents the execute portion of an instruction cycle, state in a sentence what assembly language instruction is being executed, e.g., ADD or LOAD or BRN or DJNZ or ?. (Assume the PC has already been incremented after the instruction fetch.)



The instruction is a move from memory to memory instruction, using 2 instruction words as in MOV SRC, DST

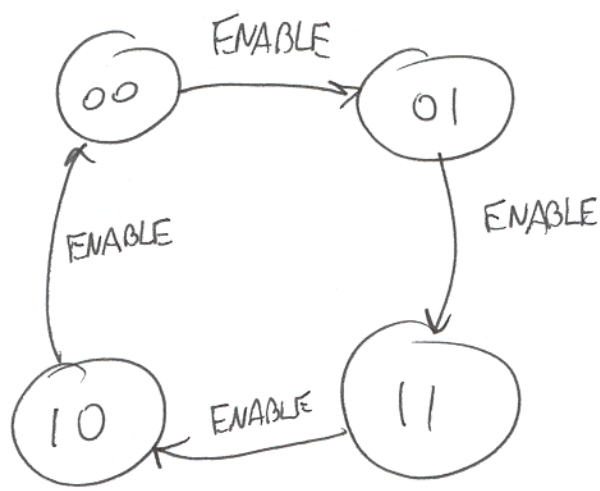
Problem 6 FSM Microprogram Analysis (12 points)

Consider the given FSM: Each FF has setup time t_{su}, hold time t_{hld}, for D and CE inputs. Propagation delay for each FF is $\geq t_{ckoMIN}$ and $\leq t_{ckoMAX}$. Inverter delay is T_{INV}. t_{su} and t_{hld} are less than 10 ns.



PS	NS
00	01
01	11
10	00
11	10

[2 pts.] **a)** Assuming proper operation, draw the state diagram for the FSM, assuming $T_3 = T_4 = 0$ ns. Use notation for the state as $(Q_1\ Q_0)$.

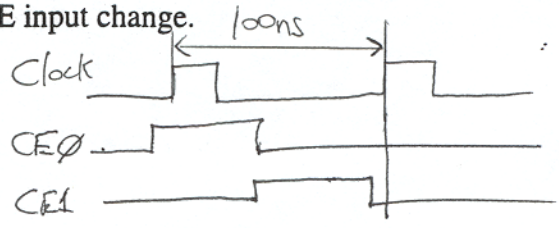


Problem 6 (cont.)

[2 pts.] **b)** With ENABLE = 1, $T_3 = T_4 = 0$ ns, what is the minimum clock period? (Express algebraically.)

period ≥ $t_{su} + t_{ckomax} + Max(T_1, T_2 + T_{inv})$

[2 pts.] **c)** With $T_3 = T_4 = T_5 = 0$ ns, $T_6 = 50$ ns, and clock period = 100 ns, an asynchronous input ENABLE lasting 50 ns is input to the FSM. Estimate the chance of violating a setup or hold time on either FF, assuming uniform distribution of the ENABLE input change.

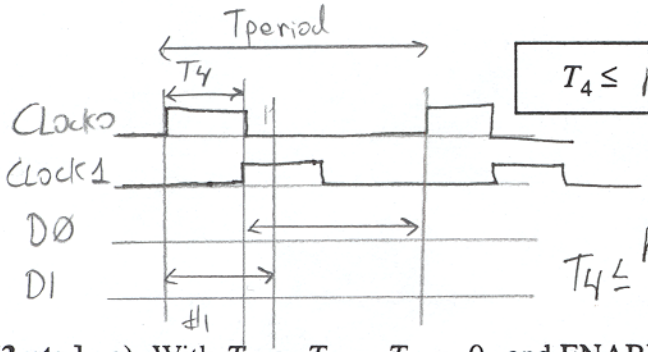


chance of violation:

either leading or trailing edge could cause setup or hold violation

$\frac{2(t_{su} + t_{hld})}{100ns}$

[3 pts.] **d)** With $T_3 = T_5 = T_6 = 0$, and ENABLE = 1, what is the maximum T_4 for proper operation of the FSM?



$T_4 \leq Min(\#1, \#2)$

Constraint #1 (hold time on FF1)

$T_4 + t_{hld} < t_{ckomin} + T_1$

$T_4 < t_{ckomin} + T_1 - t_{hld}$

$T_4 \leq \min(t_{ckomin} + T_1 - t_{hld},\ T - t_{ckomax} - T_2 - T_{inv} - t_{su})$

Constraint #2 (setup on FF0)

$T_4 + t_{ckomax} + T_2 + T_{inv} + t_{setup} < T$

[3 pts.] **e)** With $T_4 = T_5 = T_6 = 0$, and ENABLE = 1, what is the maximum T_3 for proper operation of the FSM?

$T_3 \leq$

$\min(t_{ckomin} + T_2 + T_{inv} - t_{hold},\ T - t_{ckomax} - T_1 - t_{su})$