UNIVERSITY OF CALIFORNIA

College of Engineering
Department of Electrical Engineering
and Computer Sciences

Professor Fearing | Fall 1998

EECS 150 — FINAL EXAM

Thursday, 10 December 1998, 12:30-3:30 p.m.

Name: ___________________________________ ID#: _____________

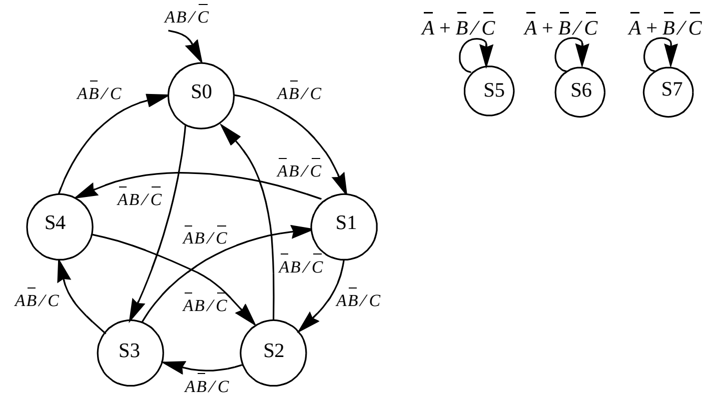
- Closed book. No notes. No calculators.
- There are 6 problems worth 100 points total. There is little room for partial credit—it's better to do half the test carefully than to do the entire test sloppily.

Problem	**Points**	**Your Score**
1	10	
2	14	
3	24	
4	10	
5	12	
6	30	
Total	100	

In the real world, unethical actions by engineers can cost money, careers, and lives. The penalty for unethical actions on this exam will be a grade of F in EECS150 and a letter will be written to the Department Chair and to the Office of Student Conduct.

Problem 1 (10 points)

Complete the state table for the Mealy-type FSM: Holding in a state is implicit. Unspecified outputs are implicitly unasserted.



Inputs A B	**Present State**	**Next State**	**Output**
0 0	**S0**		
0 1			
1 0			
1 1			
0 0	**S1**		
0 1			
1 0			
1 1			
0 0	**S2**		
0 1			
1 0			
1 1			
0 0	**S3**		
0 1			
1 0			
1 1			
0 0	**S4**		
0 1			
1 0			
1 1			
0 0	**S5**		
0 1			
1 0			
1 1			
0 0	**S6**		
0 1			
1 0			
1 1			
0 0	**S7**		
0 1			
1 0			
1 1			

Problem 2 (14 points)

[4 pts.] **a)** Find the minimal sum-of-products form for

$$Y = ABCD + ABCD + ABCD + ABCD$$
$$+ \overline{A}B(\overline{C}D + CD) + AB(CD + \overline{C}D)$$

Y = ______________________

[4 pts.] **b)** Find the minimal product-of-sums form for

$$Y = A \cdot D + AB \cdot D$$

Y = ____________________________________

[6 pts.] **c)** *State minimization.* For the following state table, determine which states are equivalent.

Present State	Input	Output	Next State
S0	**0**	**0**	**S0**
S0	**1**	**0**	**S1**
S1	**0**	**1**	**S2**
S1	**1**	**0**	**S6**
S2	**0**	**0**	**S3**
S2	**1**	**0**	**S6**
S3	**0**	**0**	**S2**
S3	**1**	**0**	**S6**
S4	**0**	**1**	**S4**
S4	**1**	**0**	**S4**
S5	**0**	**1**	**S5**
S5	**1**	**0**	**S4**
S6	**0**	**1**	**S3**
S6	**1**	**0**	**S2**

Problem 3 (24 points)

[8 pts.] **a)** Using the data path on page 8, and the timing diagram below, list in register transfer notation (RTN), the operation which is occurring on the rising edge of the clock. (Note: This timing diagram is independent of the controller on page 9.)

clock edge 1: RTN ____

clock edge 2: RTN ____

3: RTN ____

4: RTN ____

5: RTN ____

6: RTN ____

7: RTN ____

8: RTN ____

[8 pts.] **b)** The initial values for the registers are: PC = 0×2000, IR = 0×0800, AC = 0×1212. The RAM contents are:

Address	Data
0×0800	0×1111
0×0801	0×2222
0×0802	0×3333
0×2000	0×0800
0×2001	0×0801
0×2002	0×0802

Complete the timing diagram above for the Data Bus and address bus. If value is undefined, indicate by ???. Also indicate tri-state (HiZ) conditions.

[3 pts.] **c)** Assuming WE is clean, considering timing skew and possible glitches, is there a potential problem near the rising edge of clock 7? If so, briefly state the problem.

[3 pts.] **d)** Assuming WE is clean, considering timing skew and possible glitches, is there a potential problem near the rising edge of clock 8? If so, briefly state the problem.

[2 pts.] **e)** Is the memory address register needed for this design? Explain why or why not.

Problem 4 Microprogramming (10 points)

Using the data path on page 8 and microprogrammed controller on page 9, write a microprogram, in symbolic form, to execute the following algorithm: (Recall AC<15> is bit 15 of AC.)

IR → MAR
while (AC<15>=0)
{RAM [MAR] plus AC → AC, IR → MAR
 PC+1 → PC, IR → MAR}
AC → RAM [MAR]
PC → MAR
RAM [MAR] → IR

You have two micro-instructions available, DO and JMP.

Label	Operation	Comment

Problem 5 (12 points)

Using the data path on page 8, draw a state diagram(s) for a Moore-type FSM(s) which will control the following operations:

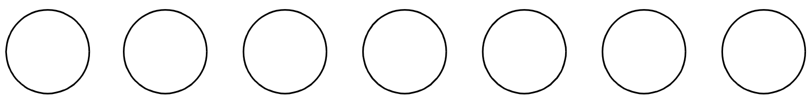
1) IR $\rightarrow$ MAR

2) AC $\rightarrow$ RAM [MAR]

3) AC plus RAM [MAR] $\rightarrow$ AC

4) PC+1 $\rightarrow$ PC

Your state diagram must show all asserted control signals and your design should tolerate timing skew without causing bus conflicts or incorrect memory operations. Explicitly show deglitching states.



Problem 6 FSM Microprogram Analysis (30 points)

Complete the timing diagram for the computer data path on page 8 and the microprogrammed controller shown on page 9. All components are synchronous. Partial microprogram ROM contents in Hexadecimal are:

Address	Hex Data
0	0×73
1	0×60
2	0×30
3	0×44
4	0×71
5	0×72
6	$0 \times E0$

The initial values for the data path registers are: PC $= 0 \times 2000$ IR $= 0 \times 0900$, AC $= 0 \times 1212$. The RAM contents are: address $0 \times 0800 = 0 \times 1111$; address $0 \times 0801 = 0 \times 2222$; address $0 \times 0802 = 0 \times 3333$; address $0 \times 2000 = 0 \times 0800$; address $0 \times 2001 = 0 \times 0801$; address $0 \times 2002 = 0 \times 0802$.