EECS 150 Final Project Report Guidelines

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Due Date

- Friday, December 3, 1999, 4pm
- Hand in unwrapped Xilinx boards
- Have a check ready for missing components
- Deposit check will be returned to you

Formatting

- Type it... Neat handwriting only for diagrams and drawings
- Use 8.5×11 paper (Exceptions allowed for diagrams or schematics)
- Single spaced, one inch margins, minimum 11 pt font
- Maximum of 9 pages of text
- Place figures as close to the reference as possible
- Label all figures
- Use comments and useful names for the control lines
- Be concise

Goal

- Functionality of Project
- Technical Description
- Documentation
  - State Diagrams
  - Schematics
  - Timing Diagrams
  - Etc.

Title and Abstract

- Accurate and descriptive title
- All relevant information about the final product
- Mode 1, 2, 3 specifications

Example:

This report contains the technical specifications for the Digital Image Manipulator we completed this semester. The design features three modes. < **Briefly** explain each mode. > We utilized 186 of the 196 CLBs on the Xilinx 4005E chip. Our design has a maximum clock frequency of 22MHz.

Overview

- Purpose and Functionality
  - What did you do?
  - Why did you do it?
  - How does it work? (Explanation on how to switch modes, etc.)
- Overall Block Diagram
- Description of Major Sub-Modules
  - RAM, UART, PWM/LED, Camera, Controllers, Etc.

System Description

- Data Path
  - If you were a piece of data, what path do you take through the system?
  - Module 1 to Module n
- Controllers
  - Figures of your state diagrams with proper labeling
  - Explanation of FSMs
  - Module 1 to Module n

Design Metrics

- Critical Timing Paths
- Max Clock Freq
- Number of CLBs
- Number of IOBs
- Estimated Hours for
  - Design
  - Implementation
  - Debugging

Conclusion

- Summary
- Problems encountered
- Any innovative solutions to problems
- What you learned from the project

Appendices

- Table of Pins
- Timing Diagrams for each Module
  - Label the state transitions
  - Only include **useful** portions of the simulation
- Schematics
- Chip pinouts
- Overall layout/pin connections