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Lab 1
Introduction to Xilinx Design Software

1 Objectives

The question "Is what I asked for what I wanted?" is ubiquitous in design; this lab introduces the tools we use to "ask for" designs, and the tools we use to try to answer this question. We will use software which integrates a "schematic capture" system (really just a schematic-specific drawing program) to specify designs, and a circuit simulator to estimate how those designs will behave when we build them.

We will use the student edition of Xilinx Foundation Edition 1.5, an extensive electronic CAD (Computer-Aided Design) system that allows you to enter digital circuit schematics and simulate them. The steps you will go through in this lab are:

- Start a new project.
- Draw schematic.
- Simulate it.

The Xilinx software, like most Windows programs, uses small, unclear icons for different features. However, if you hold your mouse over one of the icons for a few seconds, a little flag will pop up naming that button. The **Xilinx Foundation Project Manager** can be found on the "desktop".

2 Prelab

Things to do/know *before* coming to lab:

- **Learn Windows**: In the CS150 lab, the Xilinx software is run under Microsoft Windows NT 4.0 (it also can be run under Windows 95 and 98 for those of you that would like to attempt to run it at home), so you need to know how to use pull-down menus, move windows, get around the program and file manager, etc. Your best bet is to bother a colleague, but the TAs may also be helpful.
  Save your work often. This is your only real defense against software bugs. Saving your work often means both on the network, and onto your personal floppy disk. In the past, for periodic excitement, Windows NT and the network combined randomly to truncate files. For safety, first make sure those files you think you are copying from the network to your floppy are not corrupted. We will announce outbreaks of network flakiness, usually in November, but you don't want to be the one who finds the problem by losing half your file contents. This is good practice for the "Real World", where snafus also can't be avoided.
  Remember, **`Ctrl-Alt-Del`** is your friend (this interrupts things under Windows NT, giving you a chance to kill buggy programs, change your password, etc).
  When a particular mouse button isn't mentioned, assume the left. For example "click" usually means "click with the left mouse button".
- Read through this lab.

3 Before Getting Started

A word of warning: Really big systems like Windows and the Xilinx Foundation Project Manager are never entirely bug-free or perfectly set up, so don't be surprised when something unexpected like an incomprehensible error message comes up. The best thing to do is to click OK and hope that it is. (We are talking about problems with the software here. Never ignore error messages about your design!).

Also, as **`Ctrl-Alt-Del`** is your friend when Windows stops behaving, the **`ESC`** key can get you out of modes or actions that you would like to cancel when using the Xilinx software.

For bigger problems, when necessary, power on the computer. It should happily boot into Windows NT. Log in. Your login name should be your Cory account log in name. If you do not have a Cory account, you will need to obtain one and contact your lab TA.

4 The Software

4.1 Starting the software

To start the software. Locate the **Xilinx Foundation Project Manager** icon on the desktop and double click.

4.2 Starting a new project

Starting the software will bring up the program manager and a window that will allow you to select an existing project or create a new one. Select "**Create a New Project**" and then click on "**OK**".

The next window that comes up allows you to specify the basics of your project; Its name, location, type of design flow, libraries, type of chip, and device speed.

For this lab, use "**`lab1`**" as your project name and set the directory to your class directory:

`U:\your_username`

The values for the rest of the fields for this lab, all subsequent labs, and the project, should be:

Type: Foundation Series v1.5
Flow: Schematic
Library: XC4000E
Chip: 4005EPC84
Speed: 1

Clicking on "OK" will bring the program manager up.

4.3 The Project manager

The project manager is the base for anything you will want to do with your project. From it you can do circuit design, simulate/test your design, prepare your circuit for downloading to hardware, and quite a few other things which we will cover in future labs.

This week we will draw a circuit with the schematic editor, and then simulate it with logic simulator.

4.4 The Schematic Editor

The schematic editor is drawing software made especially for drawing logic circuits or schematics (logic circuits or diagrams will be called "schematics" throughout most of the rest of this class).

To start the schematic editor, click on the "**Flow**" tab in the right, upper panel of the Project manager, then click on the rightmost icon (an AND symbol) in the "**Design entry**" box.

Once the schematic editor comes up, you will see a column of icons on the left side of the window and a row of icons above the drawing area. The column of icons on the left contains icons for doing the actual drawing.

They are:

Select	: For selecting a component or region
Hierarchy Push/Pop	: For navigating through the hierarchy of design
Symbols Toolbox	: For adding components from included libraries such as AND gates
Draw Wires	: For drawing wires (or nets, as they are often called)
Draw Buses	: For drawing multiple wires at once as one ‘bus’
Draw Bus Taps	: For drawing wire connections to a named bus
Add Net or Bus name	: For adding additional net or bus names to existing nets or buses
Hierarchy Connector	: For designating I/O nets in symbol and macro schematics
Power Symbol	: For drawing GND and VCC symbols
Graphics Toolbox	: For drawing lines, text, circles…

Clicking on the “**Select**” icon puts you in “**select**” mode. In select mode, clicking on an item selects it, or you can drag over an area to select the area. Double clicking on a component when in the select mode brings up the component’s properties dialog, and dragging on a selected object moves it around. Delete will remove all selected objects.

The “**Symbol Toolbox**” icon brings up a dialog box with the available components listed (e.g. AND or OR gates, adders, memory components, and other more complex components). To move a component from the dialog box to your schematic, click on the component in the list that you wish to use in your schematic, then click in the work area where you want to put it down. To put down another component of the same type as one that is already in your schematic, while still in the “**Symbol Toolbox**” mode, click on the existing component, and then click where you would like to have a copy of it. To return to the “Select” mode, you can press the **ESC** key, double click on the upper left hand corner of the toolbox dialog, or click on the select icon again.

Clicking the right mouse button over the work area will bring up a menu containing the drawing functions. Clicking the right mouse button over a component, such as a AND gate, will bring up a menu containing operations on that symbol (symbols will be covered a little later in this handout).

The icons above the drawing area are for doing things not directly related to drawing. They are:

New schematic	Cut	Undo	Simulation Toolbox
Open a Schematic	Copy	Redo	Simulator
Save	Paste	Properties	Query Window
Projects	Zoom In/Out	Connect Symbol	
Print a Schematic	Zoom Area	Disconnect Symbol	
	Full Page Zoom		

Try to get used to using as many of these as soon as possible. You will be glad you did when you have to draw much larger designs later in the semester.

4.5 The Logic Simulator

The logic simulator allows you to set values to any pins or named wires in your schematic and observe the behavior resulting from setting those values. The results can be watched through the command window (a textual interface) or through the waveform viewer (which shows results in a graphical form).

To start the Logic Simulator, click on the “**Flow**” tab in the upper right panel of the Project manager, then click on the icon (an AND symbol with squiggles in a little black box on top of it) in the “**Simulation**” box.

To select signals to watch, click on the “**Select Component**” icon (See Figure 1). Double click on the signals that you wish to watch. As you double click on a signal it should immediately appear in the waveform viewer’s list of signals that are being watched.

There are two ways to set signal values; Through the “**Select Stimulator**” dialog or through the command window. Both of these will be introduced in greater detail later in this handout.

Once you have selected signals to watch and set the input values to your circuit, you can simulate your circuit’s behavior. Single step simulation can be done in the command window by typing “sim” or by clicking on the “**Simulation Step**” icon which is located under the “Window” menu.

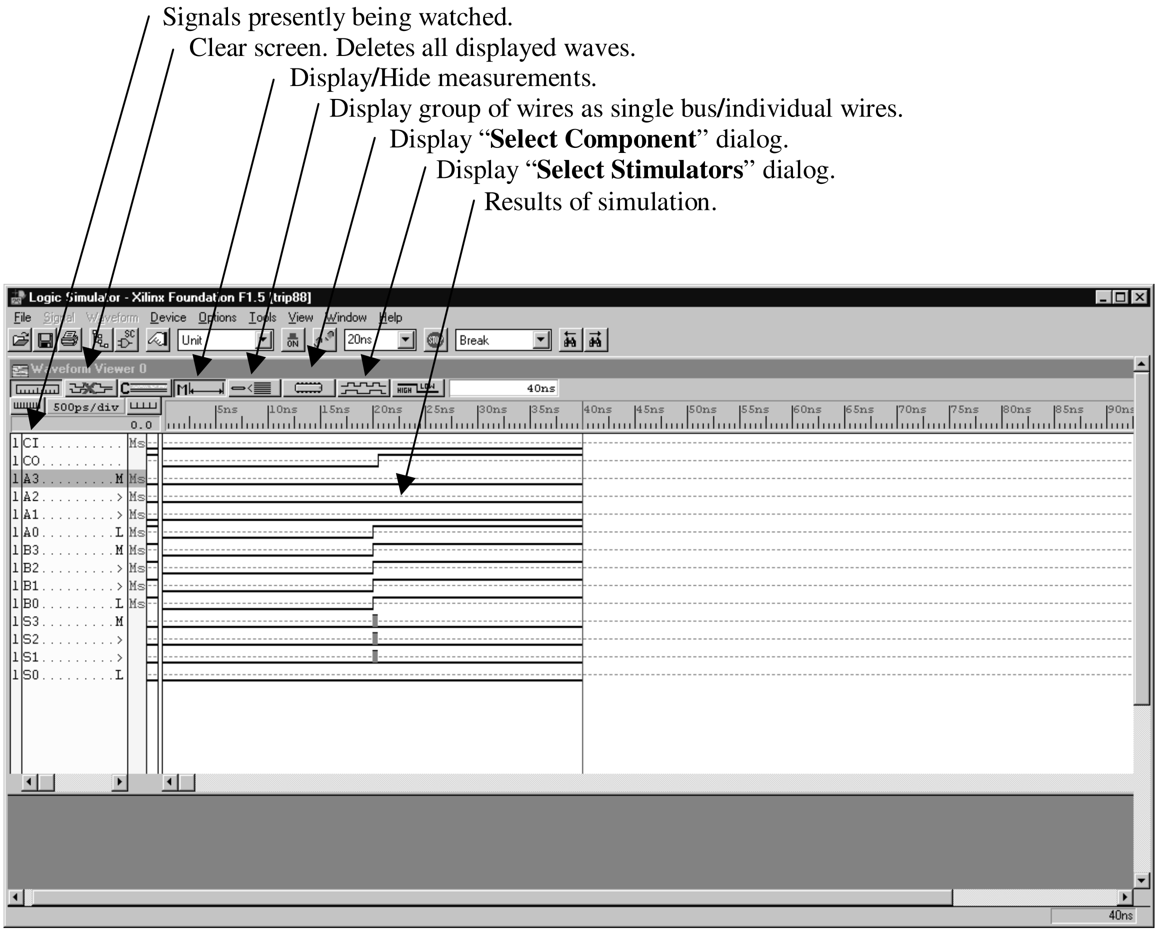


Figure 1: Logic Simulation Window

5 Entering an XOR Gate Schematic (To Do #1)

Use the Xilinx schematic editor to create a schematic for an XOR gate using Figure 2 as a guide.

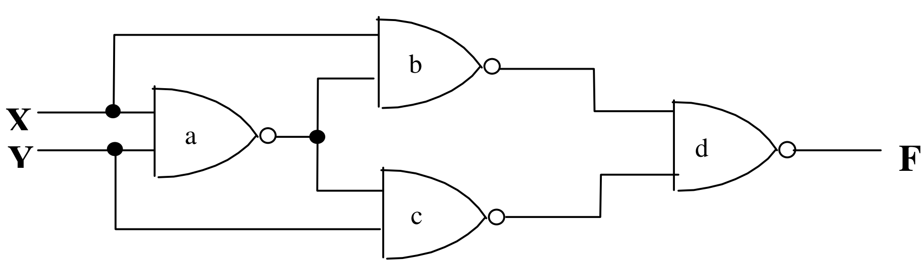


Figure 2: Schematic for an XOR

Set up:

1. Start a new project called "**Lab1**". (See 4.2 Starting a new project).
2. Start the schematic editor. (See 4.4 The Schematic Editor).
3. Open a new schematic by selecting **File → New Sheet** or by using **Ctrl+N**.
4. Save sheet to a schematic file called **MyXOR** by going to **File → Save As…**, changing the name of the file to be saved to **MyXOR.sch**, and clicking on **OK**.

Adding components :
1. Click on the **Symbols Toolbox** icon.
2. Select the NAND symbol by typing “N” in the window at the bottom of the **Symbols toolbox** or by scrolling down and selecting the NAND gate from the list with a mouse click.
3. Move the mouse pointer over to the work area and click where you want the gate.
4. Click on the NAND gate you just put down, then click where you want your next one.
5. Repeat until all four NAND gates have been put down.

Adding wires:
1. Click on the draw wires icon.
2. Here let’s connect the easiest wires first: First connect wires between gate pins, such as the wire between “b” and “d”. Click on the output pin of “b” and then click on the input pin of “d”.
3. Next connect “a” and “b”. Then connect “c” to the wire connecting “a” and “b”. (Clicking in space will allow you to put bends in the wire and clicking on a wire will attach the wires).
4. To draw the output wire “F”, click on the output pin of “d” and then click the RIGHT mouse button where you want to end the wire. Select “label” from the menu that comes up. In the window that comes up, enter the wire name “F”. Labels can be corrected or added to a wire after it has been drawn by double clicking on the wire. This brings up a dialog where you will be able to set or change the wire’s attributes.
5. You should now be able to finish drawing the rest of the schematic. You can then move wires that didn’t end up exactly where you wanted them by entering the “Select” mode and dragging the wires to where you want them. Selecting a wire then pressing delete will erase that wire.

NOTE: It is unnecessary to draw wires between everything you want connected: wires with the same name in the same schematic are connected implicitly. When this facility makes your schematic clearer, use it! In addition, a schematic may consist of multiple pages, each schematic filename ending in 1, 2 etc. Such wires are connected across multiple sheets of the same schematic. Although this is often a useful feature, it may confuse a schematic, making it harder to debug.

Saving and checking the schematic:
1. Select **File → Save** or click on the floppy icon to save file.
2. To make it possible to simulate create a netlist by selecting **Options → Create Netlist**.
3. To catch other errors before you go to simulation, run **Options → Integrity Test**. (The design for lab1 will probably not have any errors that will be caught by the integrity test).
4. You will also need to run **Options → Export Netlist**.to make it possible for other Xilinx software, such as the simulator, to access your design. If you make a change to your schematic while running the simulator, in many cases, the simulator information will be automatically updated, but when in doubt, run **Option → Update Simulation**. You will still need to export the netlist before starting new simulator sessions or when you use other software in the Xilinx suite such as the implementation software.

Printing your file:
Please save trees and DON’T print out your design for lab1.

6 Simulating your circuit (To Do #2)

Setting up the simulation of your XOR circuit:
1. Start the “**Logic Simulator**”.
2. Select the X, Y, and F signals to watch.

Simulation using "**Select Stimulators**" dialog:

1. Display "**Select Stimulators**" dialog by clicking on icon or by running **Signal → Add Stimulators…**
2. Select the X signal in the logic simulator window, then click on B0 in "**Select Stimulator**" window. B0 is the lowest bit of a 16 bit counter and alternates 0 and 1 on each half clock. Set your step size (which is displayed next to the "**Simulation Step**" button) to 50ns and your B0 period (**Options → Preferences…**) to 100ns for this lab.
3. Select the Y signal and set it to B1.
4. Step through a number of cycles by using the "**Simulation Step**" button.

Simulating using the Command window:

1. Open the "**Command Window**" (**Window → Command Window**).
2. Erase old waveforms and signals (**Signals → Delete Signals → All**).
3. Type:

```
restart
w x y f
l x y
sim
h y
sim
h x
l y
sim
h y
sim
```

'restart' sets time back to zero, and resets all signal values to unknown. 'w' adds the signals 'x', 'y', and 'f' to the Waveform Viewer, 'l' (it's an 'L', not a one) means to set the following signals to zero. 'h' means to set the signal value to one. 'sim' does the same thing as the "Simulation Step" step button does.

You can save this to a file by using the "**Tools → Script Editor**". Enter commands just as you would when using the command window, and then run the file using "**File → Run Script File**". This will be helpful when you start testing larger circuits.

7 Create a Symbol (To Do #3)

To use your XOR gate in other schematics, you need to create a symbol for it. Like the NAND gates you used, the symbol for the XOR gate will consist of a shape with some pins where nets can connect. With this symbol, your XOR gate can be used just like you used the NAND gates.

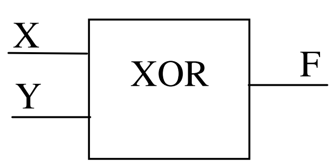


Figure 3 : Symbol for an XOR gate

There are two ways to create a symbol. The first is to use the **Hierarchy → New Symbol Wizard**, but since you have already drawn your XOR, and using the Wizard will require you to redraw, we will use the second method.

Creating a symbol:

1. Go back to Schematic editor. Bring up your MYXOR circuit.
2. Hierarchy connectors need to be added to the inputs and outputs of your schematic. You can do this from the "**Symbols Toolbox**" (top left icon in toolbox) or by clicking on the hierarchy connector icon on the left side of the Schematic Editor.
3. For X, input "X" as the terminal name and select INPUT as the terminal type. Click OK and place the terminal near the X input wire. Connect the new terminal and X with a net.
4. Do the same for Y. Also, do the same for F but make sure you set the terminal type to OUTPUT.
5. Save the new schematic.
6. Click on "**Hierarchy → Create Macro Symbol from Current Sheet**". Everything should be set, but check to make sure the inputs and outputs are correct. Press OK and you're done. You should now have a component available in your symbols toolbox called MYXOR.

WARNING: To edit a schematic for a macro use **File → Open Macro**. Editing the MyXOR schematic will **not** change the logic for your MyXOR symbol.

8 4-Bit Ripple Adder (To Do #4)

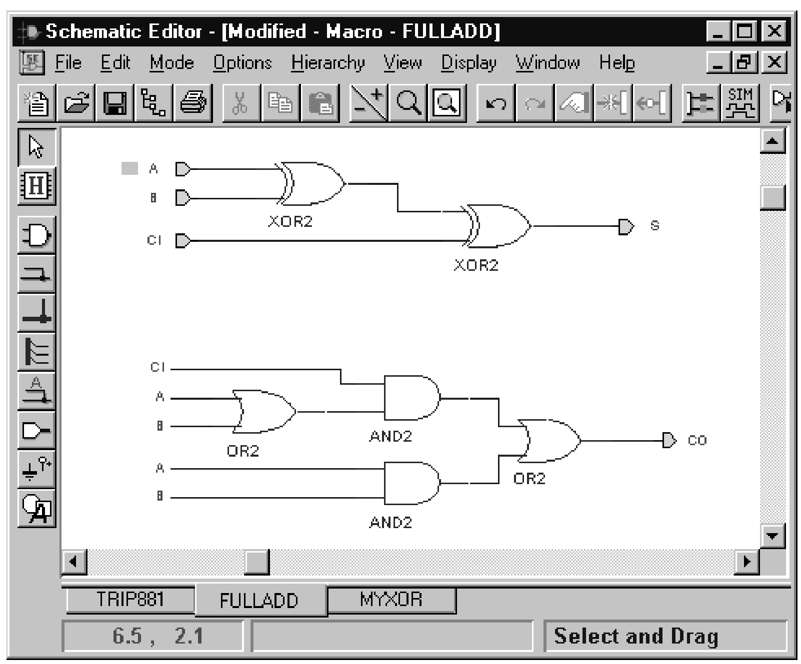
In this section, you will use the Schematic Editor to draw and simulate a full-adder. Then you will use this basic block to build a 4-bit ripple adder.

The truth table in 4a defines a full-adder. The full-adder has three inputs, A, B (two addends), and CI (carry in), and two outputs S (sum), and CO (carry out).

A multi-bit ripple adder can be built from smaller multi-bit ripple adders (a full adder). Figure 5 shows a 4-bit ripple adder built from four full-adders. A 4-bit adder adds two 4-bit numbers to produce a 4-bit result and a carry out bit. Enter the design and simulate with the data as shown on the checkoff page.

A	B	CI	S	CO
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

(a)



(b)

Figure 4: (a) full-adder truth table and (b) Schematic derived from truth table.

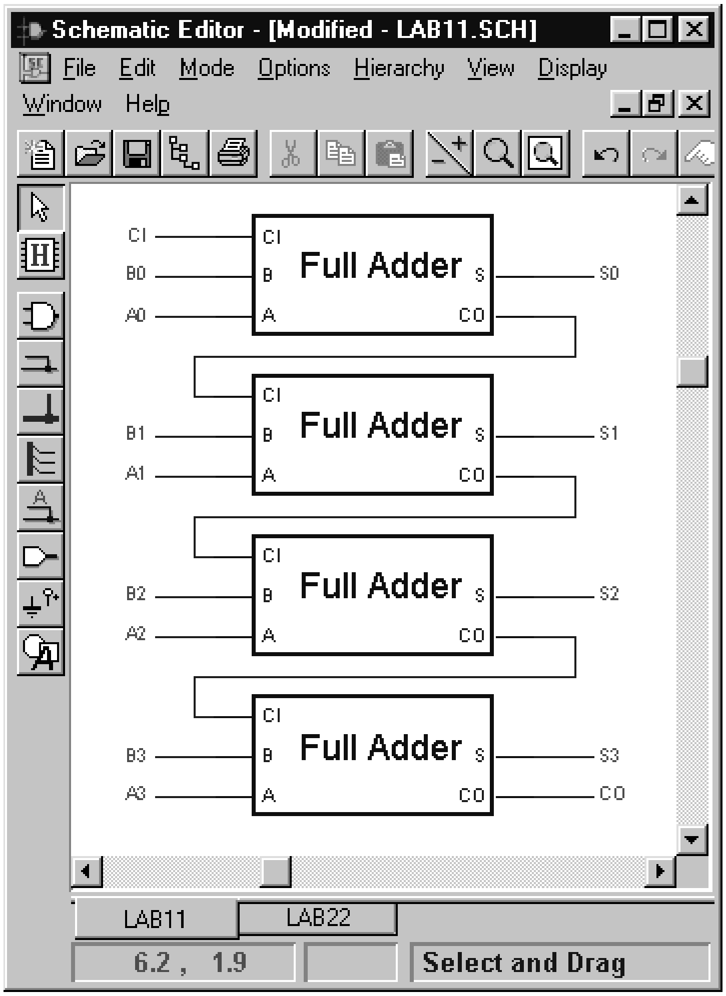


Figure 5: 4-bit adder

Name: ____

Lab Section (Check one)

M: ☐ AM ☐ PM   T: ☐ AM ☐ PM   W: ☐ AM ☐ PM   Th: ☐ PM

9 Checkoffs

To save yourself (and the TA) time, complete *all* sections below, then have the TA examine your work.

9.1 Create and Simulate a Full-Adder Cell

Figure 4b shows a typical full-adder. Enter it into the schematic editor and build a symbol for it. Bring up the simulator and simulate the full-adder to obtain a waveform representation of the truth table.

Show your TA a working full-adder.

TA: _____________(40%)

9.2 Create 4-Bit Adder

Use Figure 5 as a guide, build a 4-bit adder.

Show your TA the working 4-bit adder.

TA: _____________(20%)

9.3 Create 4-Bit Adder

Simulate the 4-bit adder for the following inputs and determine the delay through the adder for each.

NOTE: Please change simulation type from “Functional” to “Unit” (Pulldown menu directly under Option menu in simulator window), and set the simulation precision value in the **Option → Preferences…** dialog to 10ps. To measure delays, turn on measurements on (**Waveform → Measurements → Measurements on**), then, to make the measurements visible, click on the **[M |← →|]** button in the waveform viewer. Left click on the left edge of the region that you would like to measure, then left click again on the right edge to get a reading.

	Delay
0000 + 0000	__________
0101 + 1111	__________
0000 + 1111	__________
1111 + 0001	__________

What is the worst case delay for this adder?

Why do you think this is the maximum?

TA: _____________(40%)

9.4 Turned in on time

TA: _____________(full credit (100%))

9.5 Turned in one week late

TA: _____________(half credit (50% x points))