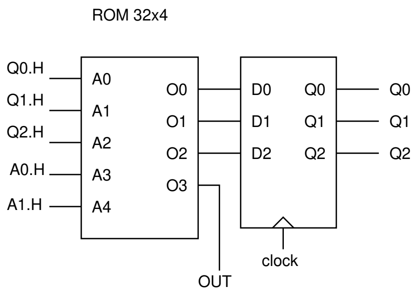
Professor Fearing EECS150/Problem Set 8 Fall 1999

Due at 10 am, Fri. Oct. 29 in box outside 218 Cory Hall

(This problem set may be done individually or by a group of two people maximum. A group of two should hand in a single copy of the solution with both names affixed). Quiz 2 in class Thurs. Nov. 4.

1. ROM Based FSM (20 pts)

Using the ROM based FSM shown below, with ROM contents as listed in Table 1, draw a state table and state diagram for the FSM. Explain why this is a Moore or Mealy type FSM. Consider synchronized inputs A1.H and A0.H. The following data is presented in order at A[1:0]: 3,1,1,1,1,1,3,0,0,0. Draw a timing diagram showing CLOCK, A1.H, A0.H, and OUT.H.



Adr	Data	Adr	Data	Adr	Data	Adr	Data
0	1	8	10	10	1	18	0
1	3	9	3	11	3	19	0
2	2	A	0	12	0	1A	0
3	B	B	D	13	A	1B	8
4	D	C	D	14	D	1C	8
5	5	D	7	15	7	1D	0
6	6	E	4	16	4	1E	0
7	6	F	6	17	6	1F	0

2. Instruction Execution (45 pts)

For the data path of Katz Fig. 11.13 (as handed out in class), a new instruction *DJNZ mem-addr brn-addr* is to be added. The instruction decrements the contents of *mem-addr* (*RAM[mem-addr] = RAM[mem-addr] - 1*) and program execution branches to *brn-addr* if the result is non-zero. The accumulator contents are unchanged.

a. describe necessary modifications to the ALU to execute this instruction.

b. List necessary register transfer operations for execution of this instruction, with associated micro-operations.

c. Show with a timing diagram the operation of the processor during the *DJNZ* instruction. Show CLOCK, all relevant control signals, data bus valid or tristate times, data bus contents, and indicate the clock edge when a particular operation occurs. (Assume WE.L is generated from a negative edge triggered D FF.)

d. Draw a state diagram for the instruction execution states assuming a Mealy FSM.

3. (35 pts)

Katz Ch. 11, problem 6.