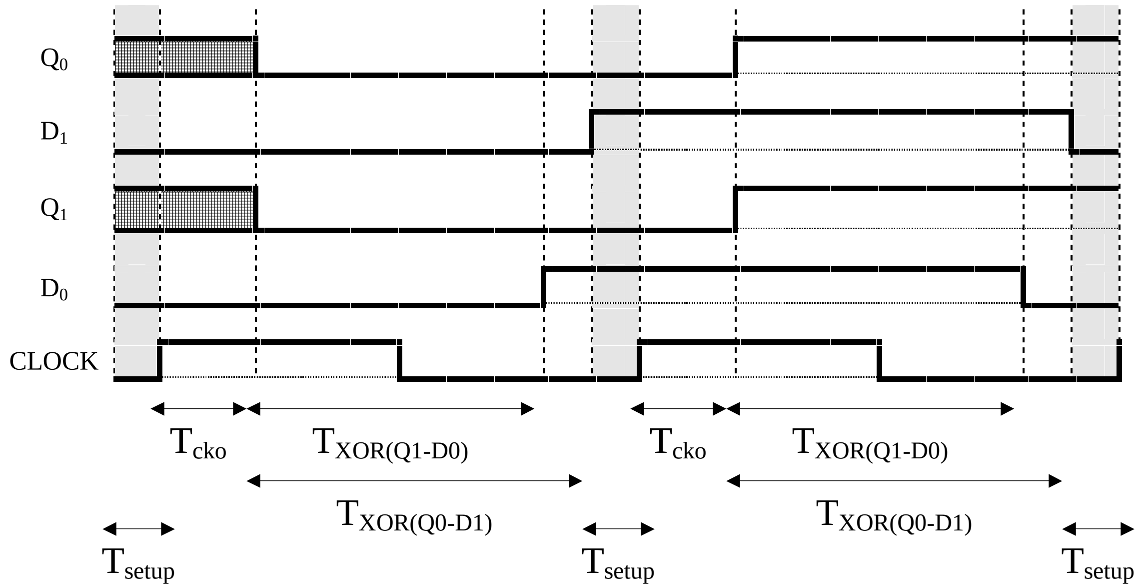
1. Synchronization (40pts)

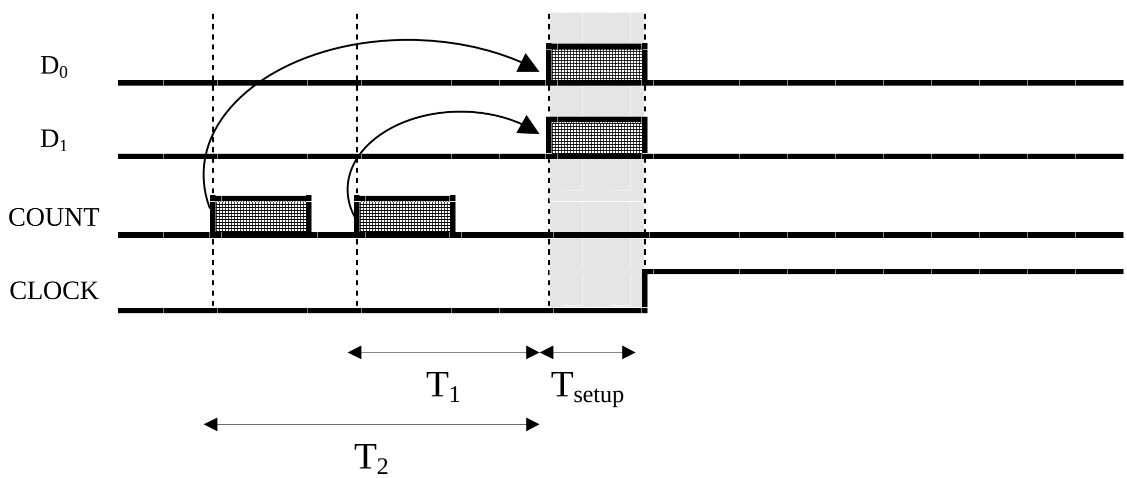
a) Initial conditions: assume COUNT is high, D_1 and D_0 are low.



min clock period = $T_{setup} + T_{cko,max} + \max(T_{XOR(Q1-D0)}, T_{XOR(Q0-D1)})$
= 6ns + 5ns + 15ns
= 26ns

So, maximum clock speed is 38.5 MHz.

b) Initial conditions: assume all signals are low. We are looking for setup time violations for D_0 or D_1.



So, assertion of COUNT between $-(T_2 + T_{setup}) < t < -T_2$,[-36ns < t < -30ns], causes a setup time violation for D_0 and between $-(T_1 + T_{setup}) < t < -T_1$,[-26ns < t < -20ns], causes a setup time violation for D_1.

c) chance of violation for a flip flop = $T_{setup} / T_{clock\ period}$ = 6ns / 100ns = 6%.
chance of violation for the whole system = $2 * T_{setup} / T_{clock\ period}$ = 12%.

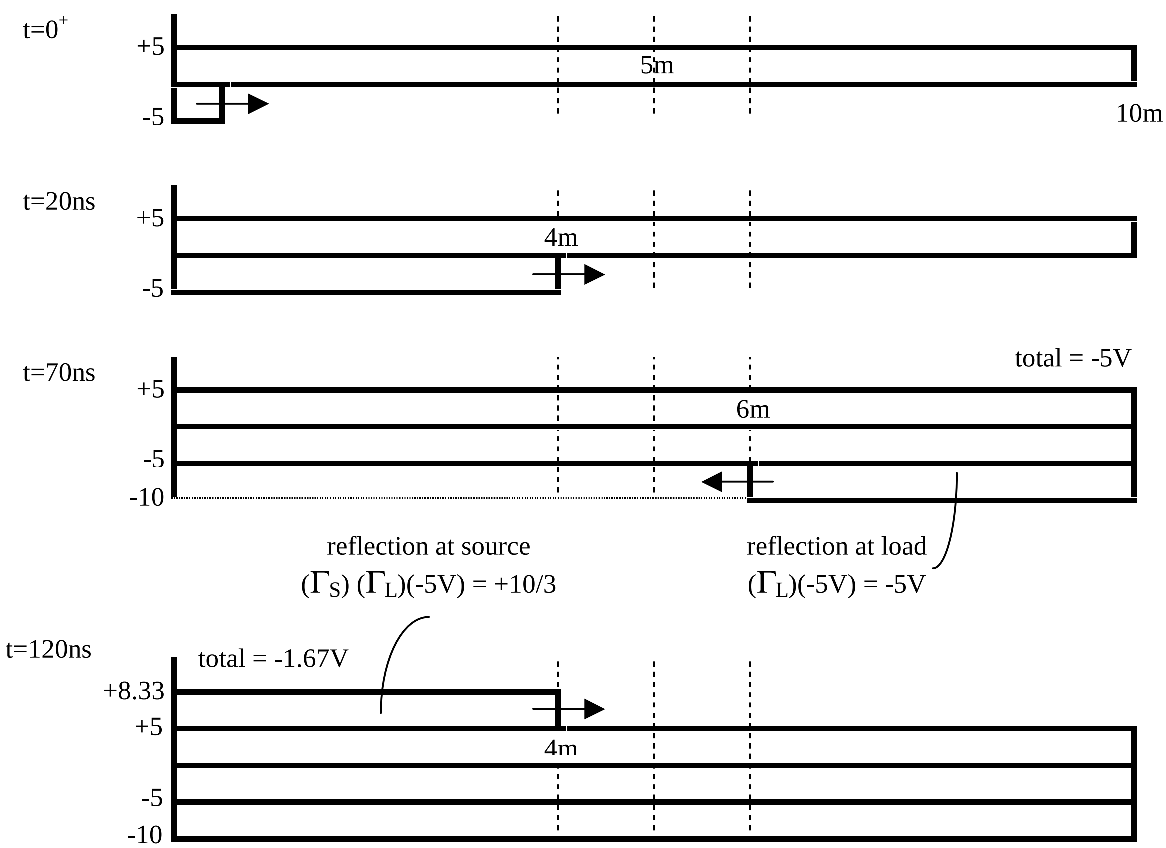
(the probability of violation for the whole system is double that of a single flip flop because the violations in part b don't overlap. So, the probabilities simply add up).

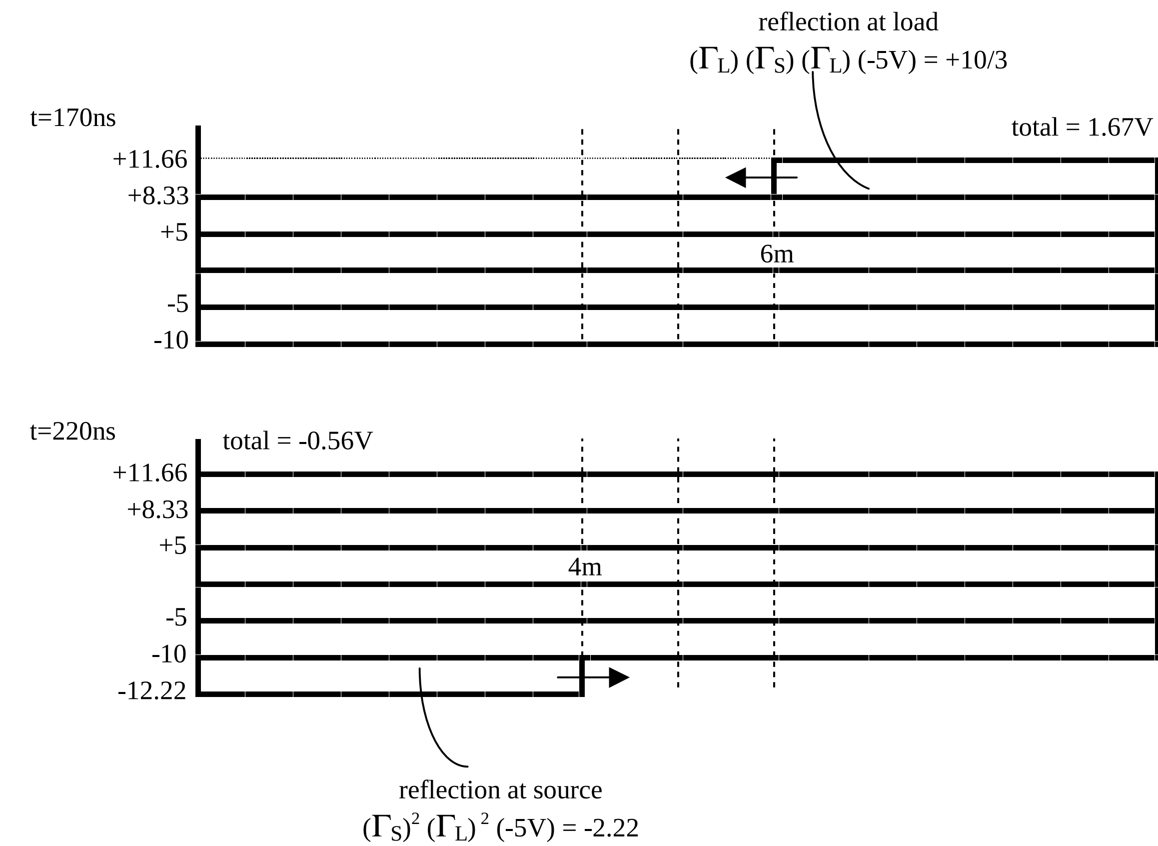
2. Termination and Reflections (25pts)

a) T_p = Length / Velocity = 10m / ($2 * 10^8\ ms^{-1}$) = 50ns.
$\Gamma_L = (Z_L - Z_O) / (Z_L + Z_O) = 10^6 - 50 / (10^6 + 50) \approx 1$.
$\Gamma_S = (Z_S - Z_O) / (Z_S + Z_O) = 10 - 50 / (10 + 50) = -2/3$.

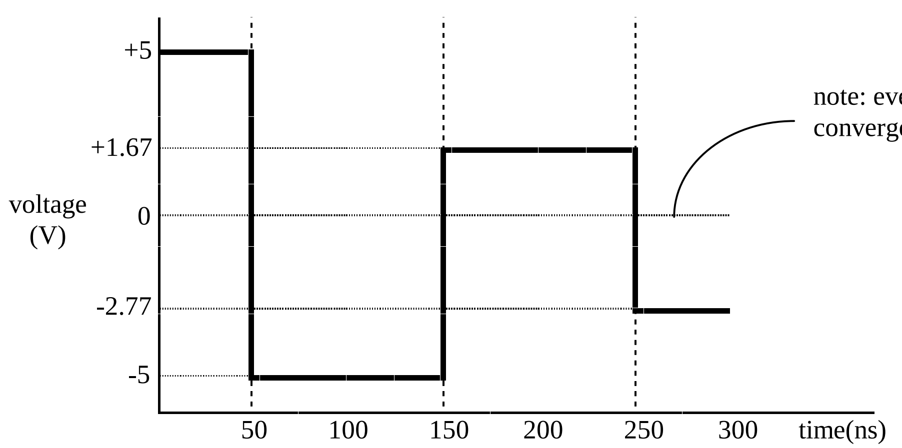
$V_f = 0V$, $V_i = 5V$, so $V_f - V_i = -5V$ wave is being sent from source to load.

Reflection pictures follow the conventions used in lecture:

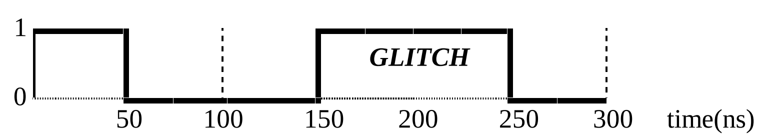




b)

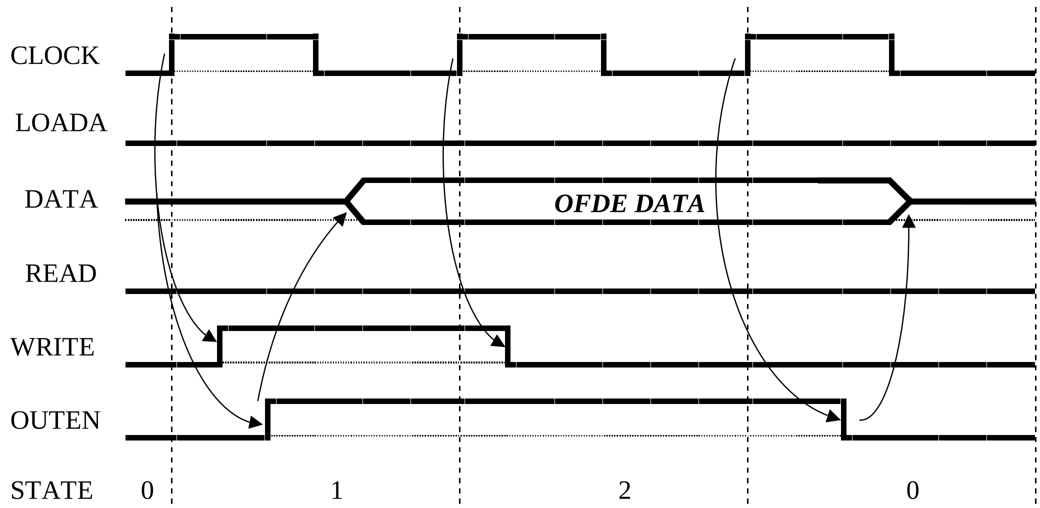


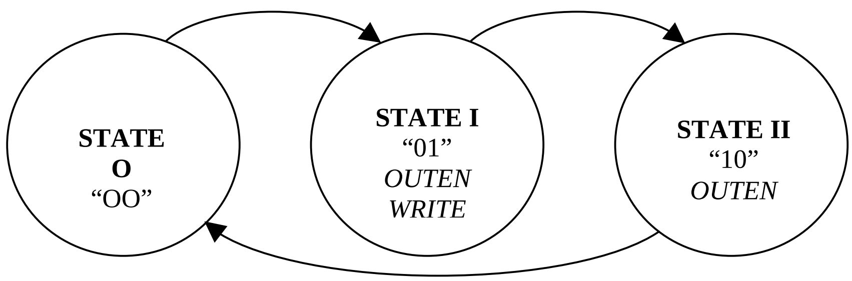
c) Reflections cause voltage to exceed threshold between 150ns and 250ns, resulting in a glitch.



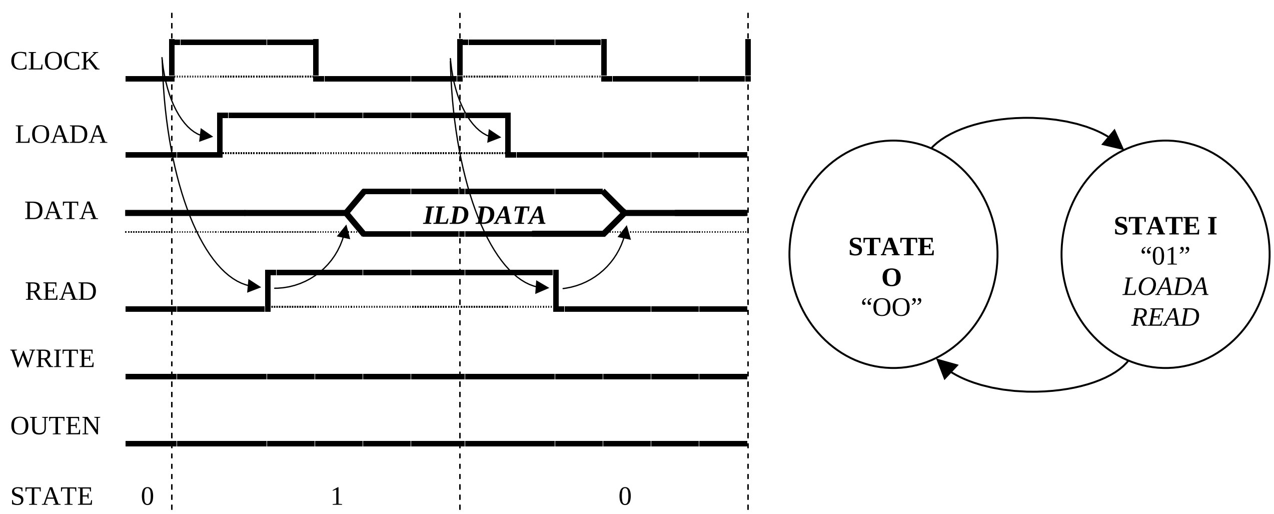
3. Xilinx Tristate IO (35pts)

a) **FSM I**





b) **FSM II**



Note: since OFDE is edge triggered, with no hold time, we don't need to assert READ for more than one clock cycle.

c) This solution uses Logic: CMOS, Device: XC4005E, Speed: -4 charts to estimate IOB timing.

Part A: Looking at the timing diagram in 3a, we need to find the worst delay during the three clock cycles:

clock cycle I: we either assert WRITE or we assert OUTEN which then sets up data from OFDE; To assert WRITE signal, we go from IPAD to G of ILD, so the delay parameter we are looking for is $T_{CKO} + T_{PDLIC} - T_{CKO} = 8.8$ns. In parallel, setting up the OFDE data into the ILD takes $T_{CKO} + T_{TSONFC} + T_{PICKC} - T_{CKO} = 9.1\text{ns} + 6.0\text{ns} = 15.1\text{ns}$, which is the time it takes to set the tristate E to active + the setup time from IOPAD to D of ILD. So, the worst delay during this cycle is 15.1ns. Note that T_{CKO} doesn't play a role in these operations, because ILD is a level sensitive latch.

clock cycle II: we deassert WRITE signal; as before this is $T_{PDLIC} = 8.8$ns.

clock cycle III: we deassert OUTEN, which then sets the data from OFDE to Hi-Z; It takes $T_{TSHZC} = 5.2$ns, to set the tristate to Pad Hi-Z.

Therefore, the minimum clock period for this FSM is 15.1ns. The operation takes three clock cycles. So,

$$T_{OPERATION} = \text{\# of clock cyles} * \text{clock speed} = 3 * 15.1\text{ns} = 45.3\text{ns}$$

Part B: Looking at the timing diagram in 3b, we need to find the worst delay during the two clock cycles:

clock cycle I: we either assert LOADA or we assert READ which then sets up data from ILD; Since LOADA is the clock enable signal, it has to be stable during setup time. The delay for this operation is $T_{CKO} + T_{ECOK}$ (setup time) = 3.7ns + 4.8ns = 8.5ns. In parallel, setting up the ILD data into the OFDE takes $T_{CKO} + T_{PIDC} + T_{TSONFC} + T_{PICKC} = 3.7\text{ns} + 5.5\text{ns} + 9.1\text{ns} + 6.0\text{ns} = 24.3\text{ns}$, which is the time it takes to assert the READ signal + IPad to tristate active time + tristate E to IOPad active time + the setup time from IOPAD to D of OFDE.

clock cycle II: we deassert LOADA or we deassert READ which then sets the data from ILD to Hi-Z. As before, the delay for deasserting LOADA is 8.5ns. In parallel, it takes $T_{CKO} + T_{TSHZC} = 3.7\text{ns} + 5.2\text{ns} = 8.9\text{ns}$, to set the tristate to Pad Hi-Z. So, the worst case delay during this cycle is 8.9ns.

Therefore, the minimum clock period for this FSM is 24.3ns. The operation takes two clock cycles, So,

$$T_{OPERATION} = \text{\# of clock cyles} * \text{clock speed} = 2 * 24.3\text{ns} = 48.6\text{ns}$$

d) The WRITE signal needs to be glitch-free because this signal determines exactly what is stored in the ILD, which is a level sensitve latch. To ensure that it is glitch-free, it needs to come from a flip-flop. The OUTEN and READ signals can have glitches at or after the rising edge of the clock, since hold time requirement is 0ns.