Professor Fearing EECS150/Problem Set 6 Fall 1999

Due at 10 am, Fri. Oct. 15 in box outside 218 Cory Hall

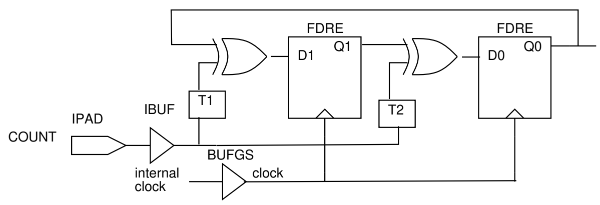
1. Synchronization (40 pts)

This question illustrates the potential problems caused by feeding asynchronous inputs into a FSM. (Even ignoring metastability). Consider the FSM below. The clock is connected using BUFGS so that there is negligible skew on the clock line. For this problem consider the parameters $T_{setup} = 6.0$ ns min, $T_{hold} = T_{CKI} = 0$ ns, $T_{CKO} < 5.0$ ns, and XOR plus interconnect (Q_1 to $D_0 = 12$ ns, Q_0 to $D_1 = 15$ ns). Delays are $T_1 = 20$ ns, and $T_2 = 30$ ns.

a. Determine the maximum clock speed using a timing diagram, showing clock, Q_0, D_1, Q_1, D_0.

b. Consider the clock signal running at 10 MHz. One of your colleagues has connected an unsynchronized input $COUNT$ to the FSM. Explain why this could be a bad idea by drawing a timing diagram, showing clock, $Q_0, D_1, Q_1, D_0, COUNT$. (I.e. show how setup time could be violated with COUNT being asserted at an inopportune time.)

c. An external system generates a high pulse on $COUNT$ lasting $100ns$. This pulse occurs at a random time (uniform distribution). Quantitatively estimate the chance of violating setup time on either FF.



2. Termination and Reflections (25 pts)

A cable of length 10 m with propagation velocity of $2 \times 10^8 ms^{-1}$ and impedance $Z_o = 50$ ohms has a driver at the transmitting end with source impedance Z_S of 10 ohms, and a load impedance Z_L of 10^6 ohms. Initally, the cable is at 5 V. At time $t = 0ns$, the transmitting driver switches to 0V.

a. Sketch the voltage along the bus at 20, 70, 120, 170, 220 ns.

b. Sketch the voltage versus time at the receiver end of the wire for the first 300 ns.

c. If the load was an IPAD/IBUF combination on a Xilinx 4005E, and the input threshold were 1.2 V, sketch the digital output of the IBUF. Is there a glitch? If so, explain why.

3. Xilinx Tristate IO (35 pts)

Consider the data path below consisting of a Xilinx output FF and a Xilinx input latch (level sensitive). For each part below, draw a functional timing diagram showing LoadA, Data, Read, Write, OutEn, and Clock, and ensure there are no bus conflicts or other problems.

a. Draw a timing diagram and state diagram for a control FSM which will write data from OFDE into the input latch ILD.

b. Draw a timing diagram and state diagram for a control FSM which reads data from ILD and stores it into OFDE.

c. Using data from the IOB timing, (p. 4-103 to 4-107) estimate how fast the operations above could be performed.

d. Which signal(s) generated by the FSM need to be glitch free? How could these glitch free outputs be generated?