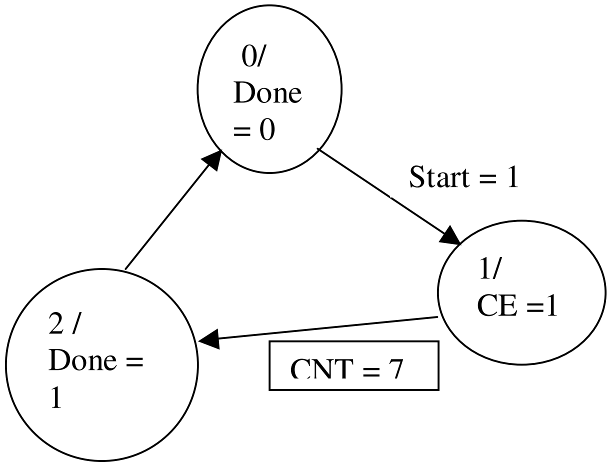
CS150 - Solutions To Problem set 4

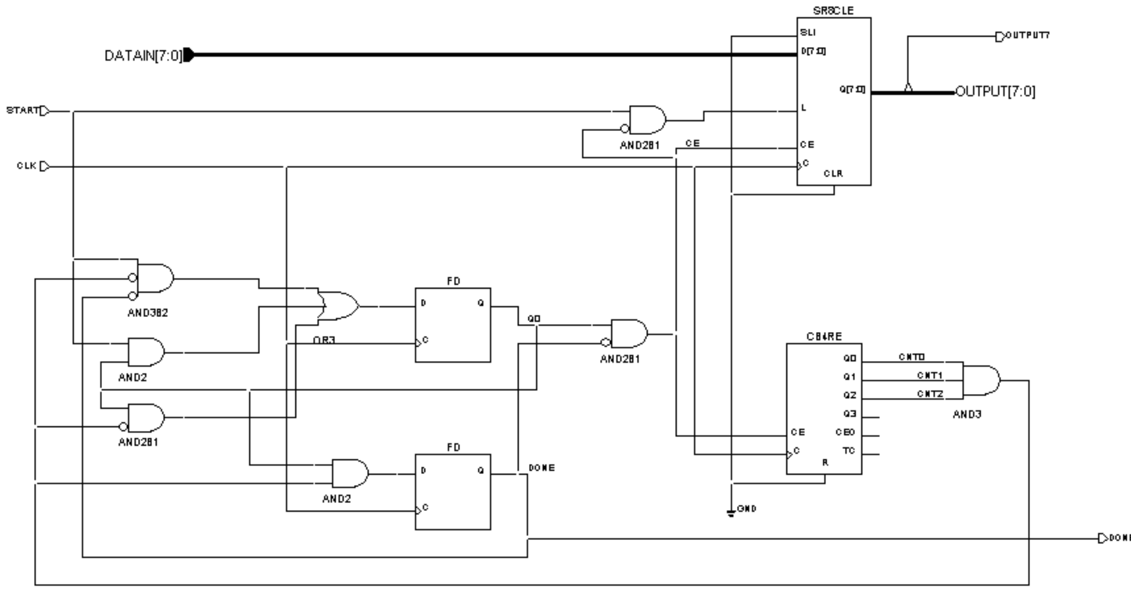
1.

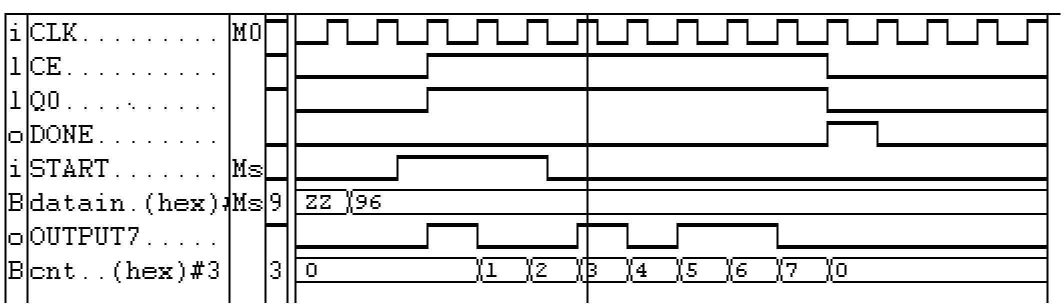


We will call CNT=7 simply C

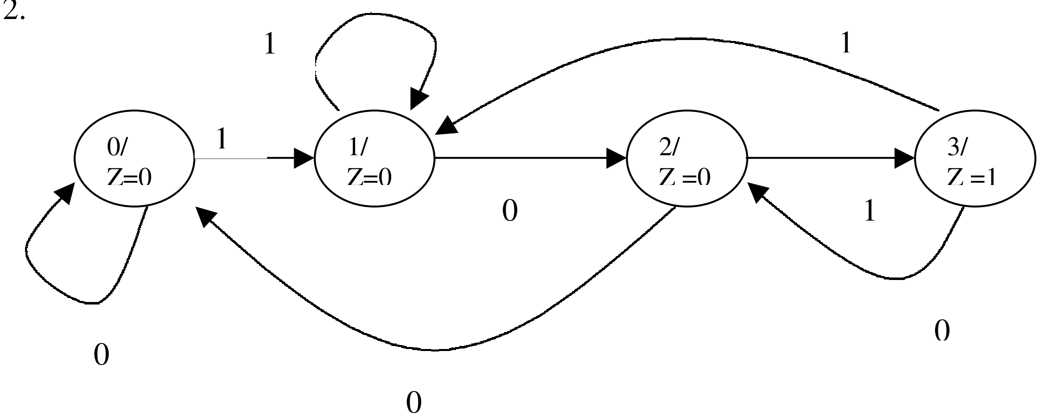
Q1	Q0	Start	C	D1	D0	CE	Done
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	1	0	0	1	0	0
0	0	1	1	0	1	0	0
0	1	0	0	0	1	1	0
0	1	0	1	1	0	1	0
0	1	1	0	0	1	1	0
0	1	1	1	1	0	1	0
1	0	0	0	0	0	0	1
1	0	0	1	0	0	0	1
1	0	1	0	0	0	0	1
1	0	1	1	0	0	0	1
1	1	x	x	x	x	x	x

D1 = Q0*C
D0 = Q1'*Start*C' + Q0*Start + D0*C'
Done = Q1
CE = Q1' * Q0


SR8CLE
DATAIN[7:0]
START
CLK
AND2B1
OUTPUT7
OUTPUT[7:0]
AND3B2
OR3
FD
AND2
AND2B1
FD
AND2
DONE
GND
CB4RE
CNT0
CNT1
CNT2
AND3
DONE


i CLK.......... M0
l CE..........
l Q0..........
o DONE.........
i START....... Ms
B datain.(hex)# Ms 9
ZZ
96
o OUTPUT7.....
B cnt..(hex)#3 3
0
1
2
3
4
5
6
7
0

2.



Q1	Q0	Z	N1	N0	OUTPUT	J1	K1	J0	K0
0	0	0	0	0	0	0	x	0	x
0	0	1	0	1	0	0	x	1	x
0	1	0	1	0	0	1	x	x	1
0	1	1	0	1	0	0	x	x	0
1	0	0	0	0	0	x	1	0	x
1	0	1	1	1	0	x	0	1	x
1	1	0	1	0	1	x	0	x	1
1	1	1	0	1	1	x	1	x	0

Where N[1:0] is the output of the JK flipflops at the next clock cycle.

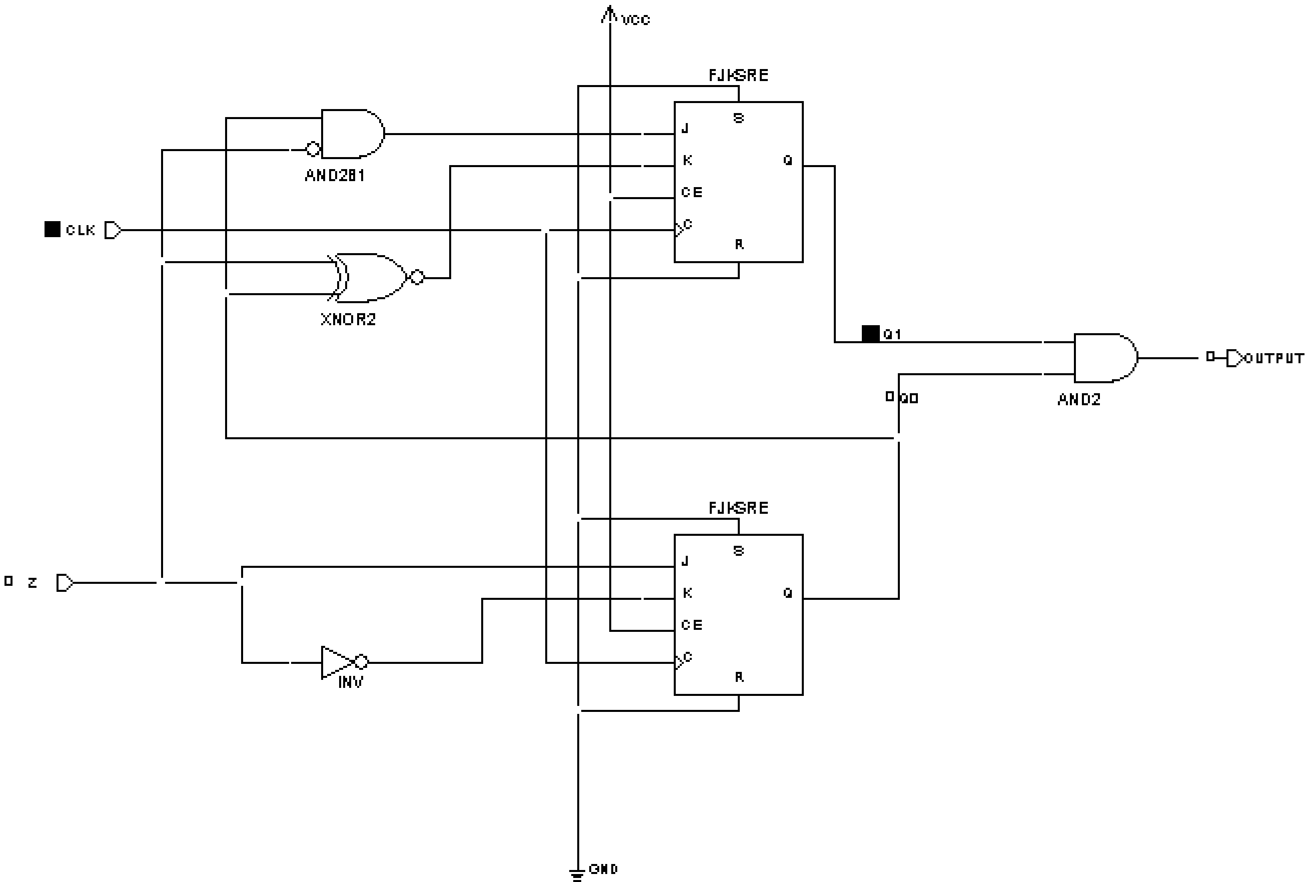
$J1 = Q0 * Z'$

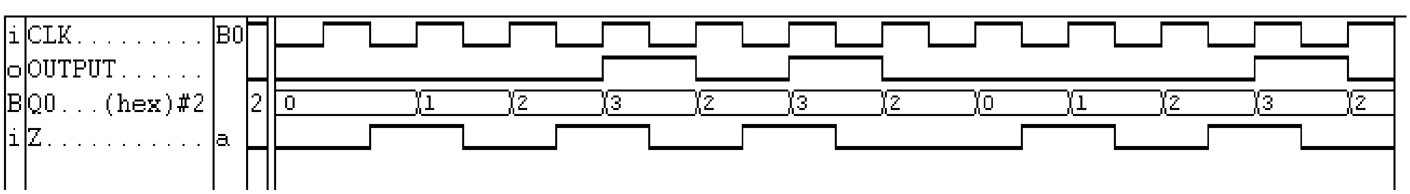
$K1 = Q0 * Z + Q0' * Z'$

$J0 = Z$

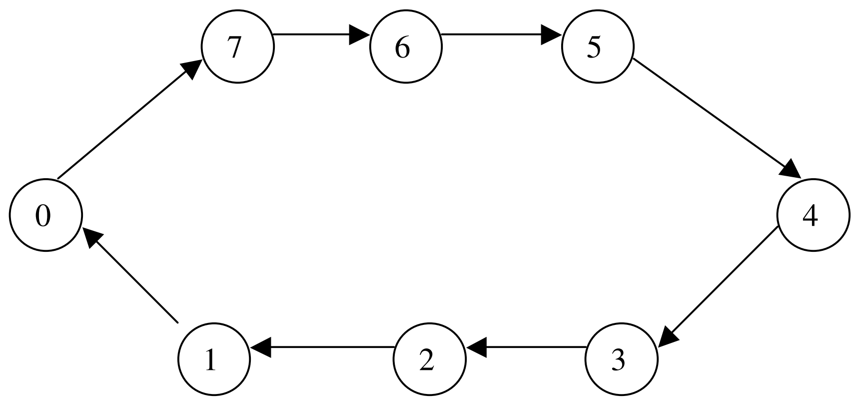
$K0 = Z'$

$OUTPUT = Q1 * Q0$


VCC
FJKSRE
J
K
CE
C
S
R
Q
AND2B1
CLK
XNOR2
Q1
AND2
OUTPUT
Q0
FJKSRE
J
K
CE
C
S
R
Q
Z
INV
GND


i CLK.......... B0
o OUTPUT......
B Q0...(hex)#2 2
i Z........... a
0 1 2 3 2 3 2 0 1 2 3 2

3.



In all states the output is the state number itself

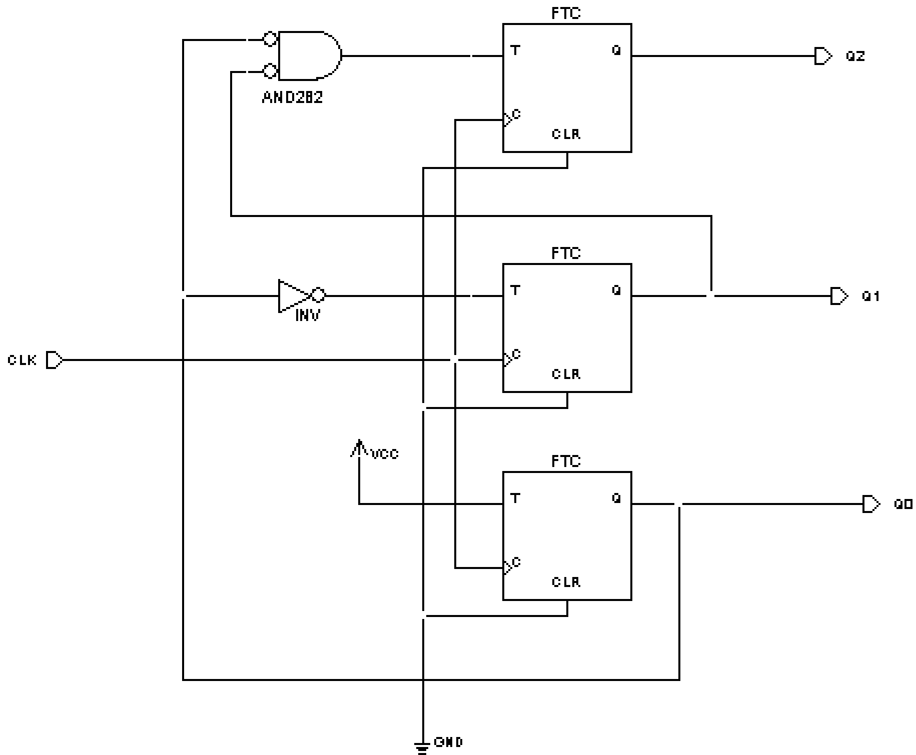
Q2	Q1	Q0	N2	N1	N0	T2	T1	T0
0	0	0	1	1	1	1	1	0
0	0	1	0	0	0	0	0	1
0	1	0	0	0	1	0	1	1
0	1	1	0	1	0	0	0	1
1	0	0	0	1	1	1	1	1
1	0	1	1	0	0	0	0	1
1	1	0	1	0	1	0	1	1
1	1	1	1	1	0	0	0	1

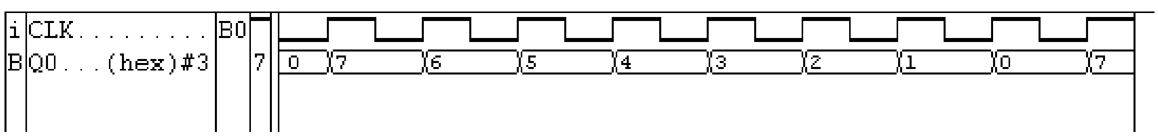
Where Q[2:0] is the present output and N[2:0] is the output at the next clock edge. T[2:0] are the inputs to the T-flops.

T0 = 1

T1 = Q0’

T2 = Q0’ * Q1’


FTC
T
Q
C
CLR
Q2
AND2B2
INV
Q1
CLK
VCC
Q0
GND


i CLK.......... B0
B Q0...(hex)#3 7
0
7
6
5
4
3
2
1
0
7

4.
Minimum Period -
T_{min} = max {T1, T2} where
T1 > Tcko1 + Del1 + Tsetup2 = 20 + 10 + 15 = 30 ns
T2 > Tcko2 + Del2 + Tsetup1 + Tinv = 20 + 5 + 15 + 18 = 58 ns

T_{min} = max {T1, T2} = max {30, 58} = 58 ns

**Note that we use the max values in all the above calculations because we want a clock that for worst-case scenarios, not best.

Fastest Inverter -
We must satisfy the hold time for FF1
Tdel2 + Tinv + min(Tcko2) > Thold
As the problem is stated, there any speed inverter will work. However, if FF1 and FF2 have slightly different Tcko's then there could be a problem . In particular if Tcko2 is very fast we could have :
Tdel2 + Tinv > Thold
Tinv > Thold – Tdel2 = 8 – 5 = 3ns. So the inverter must be slower than 3ns. Tinv > 3ns.