Professor Fearing EECS150/Problem Set 4 Fall 1999

Due at 10 am, Fri. Sep. 24 in box outside 218 Cory Hall

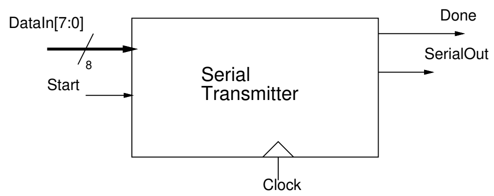
Quiz 1. 2-330 pm Tues. Oct. 5, 10 Evans

Reading Katz: 6.1:6.3,8.5, 10.4

1. Parallel-to-Serial Converter (35 pts)

Design a system which can convert 8 parallel input bits (DataIn[7:0]) to a serial output SerialOut. The system operates as follows. A clock signal is provided which is synchronized with DataIn[7:0]. When START is asserted, the system should first load the 8 bits, then shift out 8 bits (one bit per clock cycle), then stop shifting and assert the DONE signal. The data path of the system should use an 8 bit shift register and 3 bit counter from the Xilinx library, and any other necessary combinational logic. (The 3 bit counter keeps track of when 8 bits have been shifted out). The control section should use a D FF based Moore FSM to keep track of whether the system is waiting for START or shifting.

In addition to schematic, show a timing diagram of operation, and state diagram for the controller FSM.



2. FSM Design (20 pts)

Design a Moore type FSM for a sequence recognizer. The FSM should assert OUTPUT for one clock cycle for every (possibly overlapping) sequence "101" detected in the synchronized input data stream Z. Show timing diagram, state diagram, state table, and schematic using synchronous reset JK-type FFs from the Xilinx library (FJKRSE).

3. FSM Design (20 pts)

Design a counter, using T type FF which counts in the sequence 7,6,5,4,3,2,1,0,7,6,5,...
Show state diagram, state transition table, and schematic diagram.

4. Timing Analysis (25 pts)

Using a timing diagram, determine the minimum clock period for this circuit. (Parameters: T_{setup} = 15 ns min, T_{hold} = 8 ns, $5 < T_{CKO} < 20$ ns, T_{delay1} = 10 ns, $T_{delay2} = 5ns$, and inverter propagation $12 < t_p < 18$ ns.) Also, determine the fastest inverter which could be used in this circuit (i.e. if the inverter were faster than 12 ns, is there any potential problem?)