Professor Fearing EECS150/Problem Set 3 Fall 1999

Due at 10 am, Fri. Sep. 17 in box outside 218 Cory Hall

Reading Katz: 7.1:7.3, 10.3.4, lab reader: XC4000E p.4-9 to 4-11, 4-21 to 4-22, 4-29 to 4-35

1. Counter Design (15 pts) (more practice)

Using 3 type D flip-flops and extra logic, design a 3 bit counter which counts in the sequence $Q_2Q_1Q_0 = 0, 1, 2, 5, 3, 6, 4, 0, ...$ Show state diagram, state transition table and schematic diagram.

2. Look Up Tables (25 pts)

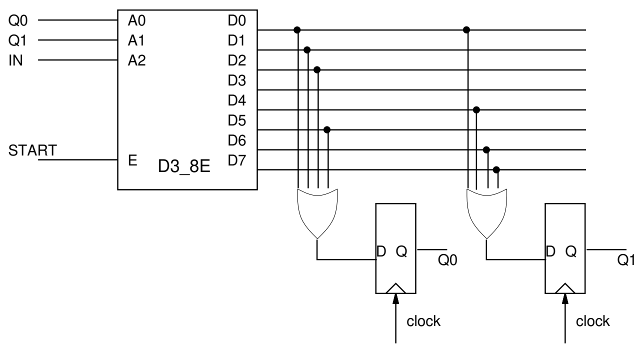
You are given a look up table (LUT) with 3 binary inputs and one output.

a) Show how these 3 input LUTs can be combined to perform ANY 4 input logic function.

a) Show how these 3 input LUTs can be combined to perform ANY 5 input logic function.

3. FSM Analysis (25 pts)

Determine the state transition table and draw the state diagram for this FSM:



4. D-FF Timing (35 pts)

Draw a timing diagram for the circuit below, assuming unit delay through the gates, and showing signals $clock, D, Q_1, Q_2, Q_a, Q_b, S, R$.